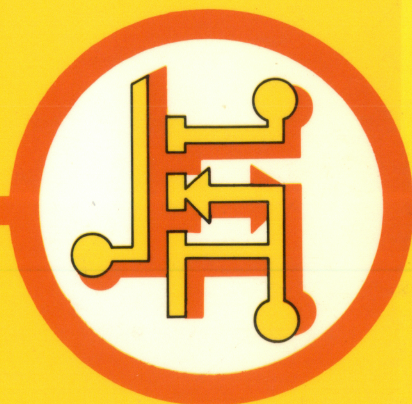
Technical Handbook

MOSFETS



FERRANTI
Semiconductors

Issue 3, November 1985 R1M

Printed in England HK&R

Mosfets Technical Handbook

Since publication of this Ferranti Mosfets Technical Handbook the following data sheets have become available:

Industry Standard	**BS250P**
ZVP21 Range	**ZVP2106A/B/L**
	ZVP2110A/B/L
	ZVP0120A/B/L
ZVP33 Range	**ZVP3306A/B/F**
	ZVP3310A/B/F
	ZVP1320A/B/F
ZVN33 Range	**ZVN3306F**
	ZVN3310F
	ZVN1320F

For upto date information on Ferranti Mosfet data please contact your nearest Ferranti sales office.

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INTRODUCTION

This product guide contains data on the Ferranti range of N and P channel MOSFETS as well as a selection guide and cross reference index.

New Products

The continual evolution of new products means that the Ferranti range is being constantly updated. If your particular requirement is not covered within this book, please do not hesitate to contact us for new product information.

Applications Laboratory

An experienced team of applications engineers is available to give advice and active assistance with circuit design and system problems.

Customer Specifications

Devices may be supplied against 'in-house' Ferranti specifications to suit individual customer requirements for non-standard electrical specifications.

MOSFET Dice

Ferranti MOSFETs are available in wafer or individual dice form.

FERRANTI MOSFET TECHNOLOGY

TECHNOLOGY SUMMARY

Ferranti MOSFET technology is amongst the worlds most advanced. Our NEW generation of MOSFETs offer today the performance required for designs of tomorrow.

Ferranti MOSFETs utilize a vertical DMOS structure. These devices are produced using a well proven silicon gate manufacturing process which provides excellent device stability under high voltage conditions. Low input capacitance and fast switching speeds are achieved by virtue of the chips having either overlay (cell) or interdigitated geometries. In common with all MOSFET devices they do not exhibit thermal runaway or thermally induced secondary breakdown.

Ferranti MOSFETs are enhancement mode FETs (normally-OFF) especially suited to a wide range of switching and amplifying applications where high input impedance, high gain, high frequency and fast switching speed is desired. They combine the current handling capabilities of bipolar transistors with the high input impedance and negative temperature coefficient of FETs.

FERRANTI VERTICAL DMOS STRUCTURE

Having considered the various MOSFET technologies, Ferranti has chosen a vertical DMOS structure (see Fig. 1).

As with other vertical current flow devices, an N^- epitaxial layer is grown on an N^+ substrate. A series of P^- body regions are next diffused into the epi-layer. Then N^+ source regions are diffused within the P^- body regions and a polycrystalline silicon gate is embedded in the silicon oxide insulating layer. Source and gate metallizations are deposited on the top surface of the die and the drain contact made to the bottom surface. The vertical DMOS process may be considered as truly planar as both source and body regions are diffused through a window opened in the oxide layer without grooves of any kind.

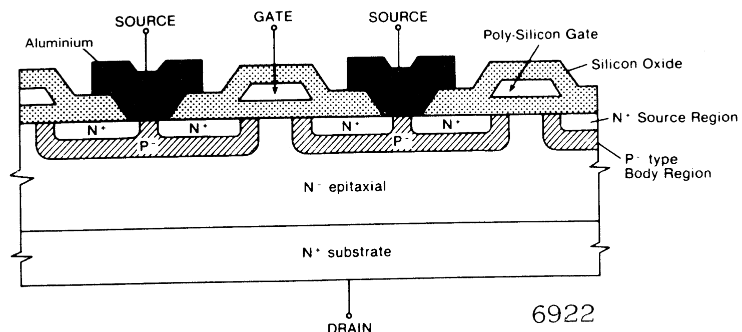


Fig. 1 Cross-Section of Ferranti Vertical DMOS Structure

FERRANTI MOSFET TECHNOLOGY

With the device turned on, carriers flow laterally from the source to the drain region below the gate and then vertically to the drain contact.

An abundance of terms already exist for individual manufacturers' versions of the basic vertical DMOS process, e.g. HEXFET®, SIPMOS®, TMOS®. The main differences between various manufacturers' products are in the geometry of the P and N regions and the interconnections. Vertical DMOS transistors can be fabricated with either interdigitated access or with a dual-access (overlay or cell) geometry. Both N-channel and P-channel devices utilize a vertical DMOS process. It should be realized however, that since the resistivity of P-type silicon is much higher than that of an N-type silicon, P-channel devices require a larger active area to achieve the same on-resistance and current rating.

For complementary symmetry, equal $R_{DS(ON)}$ is needed in both devices. Thus the P-channel device used must have a larger active area than the N-channel device. The larger area will mean that parameters related to die area will, as expected, be different; preventing symmetry in this respect.

The Integral Reverse Diode of P-channel devices will have a higher forward voltage drop than the diode in the N-channel transistor.

Advantages of a vertical DMOS structure over V or U-groove structures may be summerized as:

1. Short channel lengths determined by easily controlled diffusion process for lower ON-resistance and increased current density.
2. Planar construction simplifies wafer fabrication due to elimination of etched grooves.
3. Increased conductance per unit area.
4. Improved high voltage capability.
5. Both N and P-channel devices can easily be fabricated.
6. Compact metallization for reduced chip size.

FERRANTI PROCESS HIGHLIGHTS

- **Poly-Silicon Gate Process**
  The poly-silicon gate greatly reduces the possibility of sodium-ion contamination in the gate oxide - giving high stability of threshold voltage.
- **Ion-implantation**
  The use of ion implantation gives stability in the control of threshold voltages in manufacture.
- **Self-Aligned Gate**
  The self-aligned DMOS process allows extremely short channel lengths to be achieved, giving these devices excellent linear transfer characteristics.
- **Planar Construction**
  The vertical DMOS structure eliminates the need for anisotropically etched V or U-grooves in the surface of the device, giving improved performance and higher voltages.
- **Compact Geometries**
  Compact transistor chip designs, utilizing overlay (cell) or interdigitated structures, optimised for low ON-resistances, low capacitances and fast switching speeds.

SOURCE TO DRAIN INTERNAL DIODE

In N-channel devices the source metallization overlaps the P^- and N^+ regions which effectively short-circuits the base and emitter of the parasitic bipolar transistor, keeping it inactive and stabilizing the threshold voltage of the MOSFET. The result of this is equivalent to a P-N junction diode connected between source and drain in parallel with the MOSFET (see Fig. 2).

When the source is made positive with respect to the drain, the diode conducts with a forward current rating equal to the drain current rating of the MOSFET. In the reverse direction, the diode has a breakdown voltage equivalent to the drain-source breakdown of the MOSFET. The diode is inherently fast and can be used as a rectifier or an inductive energy clamp in switching circuits.

The internal diode of P-channel devices exhibits a forward voltage drop of several volts and is generally considered unusable.

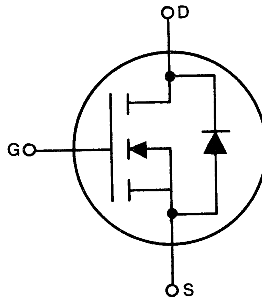


Fig. 2 N-channel MOSFET with Internal Diode

HANDLING AND PRECAUTIONS

HANDLING AND CIRCUIT CONSTRAINTS

MOSFETs, with relatively high input capacitances requiring a large charge to build up a high voltage on the gate, are less susceptable to damage from electrostatic discharge than CMOS integrated circuits. However, it is considered good practise to adopt several standard precautions, listed below, when handling the devices.

- MOSFET devices are supplied in anti-static packages and should either be retained in these or similar conductive housings until they are required for use.
- MOSFET devices should be handled by the package not the leads.
- The work stations where MOSFETs are handled should have grounded conductive floor and table mats.
- Personnel should be grounded whilst handling MOSFETs.

The above precautions should also be taken when inserting devices into circuit boards and in addition soldering irons should be grounded.

One of the most important advantages of a MOSFET is the ease with which it can be driven. The capacitive input only requires sufficient charge to develop a gate-source voltage greater than the threshold level for the device to turn on.

The input of a MOSFET is seen as a capacitor with a silicon oxide dielectric and as with all capacitors has certain parameter limits. To turn on the device fully a gate source voltage of 10V is required, however, it is important that the maximum rating of $\pm 20V$ is observed. Exceeding this level, even for a short period of time, can cause punch through of the dielectric; leading to degradation or failure of the device.

Another situation one should be aware of is voltage transients being applied to the gate as a proportion of the transient voltages occuring at the drain, suitabley potted down by the device capacitances. This is most likely when the drive circuit presents a high source impedance. Voltage transients on the supply rails can also be fed to the gate via the drive circuitry. As a precaution against voltage transients, it is recommended that a suitable zener diode be fitted between the gate and source. The increased ruggedness of MOSFETs has prevented the need for manufacturers to supply a built-in zener diode as was done originally. There were cases when the built-in zener was inconvenient as its reverse characteristics limited negative gate voltages to that of a forwardly biased diode.

Drive circuits should not normally allow the gate impedance to rise to very high values or there may be a build-up of gate voltage due to the presence of switching transients. However providing the gate voltage is controlled, circuits can be used which apply a short duration positive pulse to turn on the transistor and at a later time apply a short duration negative pulse to extract the charge from the gate and turn off the device. The retained charge in the gate holds the device in the conducting state during the interval between pulses.

One advantage of the MOSFET is its ability to switch current at a very fast rate. It is, in many ways, akin to an R.F. transistor and this must be considered when connecting the device to other circuitry. If the device is measured on a curve tracer, it is wise to ensure that the jig into which it is inserted contains a resistor, connected in series with and close to, the gate of the device under test. If the gate lead connected in the circuit, needs to be of any length, a similar resistor should be inserted. A value of 100Ω is enough to prevent parasitic oscillations causing incorrect operation or failure.

HANDLING AND PRECAUTIONS

The very good frequency performance of MOSFETs means, again like the R.F. transistor, some consideration must be given to the layout of the circuit used. Earthing leads should be minimal to reduce parasitic inductance and prevent unwanted voltage transients and in the case of fast switching circuits, to minimise ringing after fast voltage transitions.

Finally parameter limitations such as Maximum Power Dissipation, Maximum V_{DS} and Maximum I_D as given in the data sheets, must be observed.

MOSFETS versus BIPOLAR TRANSISTORS

ADVANTAGES OF MOSFETs OVER BIPOLAR

- **DO NOT EXHIBIT THERMAL RUNAWAY OR THERMALLY-INDUCED SECONDARY BREAKDOWN**

  Carrier mobility in a MOSFET channel region decreases with temperature. If localized heating occurs in a MOSFET, the carrier mobility decreases in the region affected, and as a consequence, the localized current reduces. This negative feedback mechanism forces overload currents to be uniformly distributed within the transistor.

- **HIGH INPUT IMPEDANCE AND HIGH GAIN**

  By virtue of the insulated gate structure, input currents are very low, typically a few pico amps at 25°C. Current gains are generally in the range 10^5 to 10^6.

- **LINEARITY OF TRANSFER CHARACTERISTICS**

  Above the threshold voltage the relationship between the drain current and gate voltage in these short channel devices is approximately linear. In other words the device transconductance, which is the rate of change of drain current with gate voltage, becomes constant at high drain currents.

- **TEMPERATURE STABILITY**

  The transconductance and switching times of these MOSFETs change very little with temperature compared to bipolar transistors.

- **FAST SWITCHING SPEEDS**

  MOSFETs are majority-carrier devices, and consequently do not exhibit minority carrier storage delays. Switching times are ultra-fast, primarily being determined by the device capacitances and the drive circuitry.

- **EASE OF PARALLEL OPERATION**

  MOSFETs can easily be connected in parallel to obtain very high current handling performance without the problem related to bipolar technology, that of base current sharing resistors. Additionally, paralleling MOSFETs results in the reduction of effective ON-resistance.

- **SIMPLIFIED DRIVE AND PERIPHERAL REQUIREMENTS**

  Less peripheral components are required than in the case of bipolar types leading to reduced design time, less complexity and lower cost.

MOSFETS versus BIPOLAR TRANSISTORS

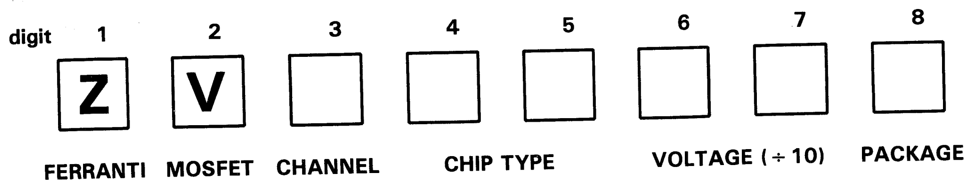
- **TERMINOLOGY COMPARISON**

BIPOLAR	MOSFETs
Collector	Drain
Base	Gate
Emitter	Source
I_C	I_D
BV_{CES}	BV_{DSS}
$V_{BE(on)}$	$V_{GS(th)}$
I_{EBO}	I_{GSS}
I_{CES}	I_{DSS}
$R_{CE(sat)} = \frac{V_{CE(sat)}}{I_C}$	$R_{DS(on)} = \frac{V_{DS(on)}}{I_D}$
h_{fe}	g_{fs}
C_{ib}	C_{iss}
C_{obo}	C_{oss}

PRODUCT INFORMATION

PRODUCT IDENTIFICATION CODES

Ferranti MOSFETs are identified by an 8 digit alpha-numeric code which is read as follows:



1st digit: Ferranti identification - Z

2nd digit: Vertical DMOS Process - V

3rd digit: Channel - N

- P

4th and 5th digits: Chip Type 01/21

22

05

13/33

14

6th and 7th digits: Voltage Rating divided by 10

e.g. 02 = 20 volts

10 = 100 volts

17 = 170 volts

24 = 240 volts

8th digit: Package code

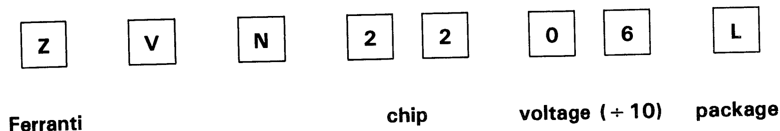
A - E-Line (TO-92 style)

B - TO-39

L - TO-220

F - SOT-23

EXAMPLE:



This number refers to an N-channel ZVN22 product family with Breakdown Voltage (BV_{DSS}) of 60 volts in a TO-220 package.

ALPHA-NUMERIC PRODUCT LIST

DEVICE	DATA SECTION	DEVICE	DATA SECTION
BS107P	1	ZVN1308A	5
BS107PT	1	ZVN1308B	5
BS170P	1	ZVN1320A	5
BS250P	REFER	ZVN1320B	5
VN10LP	1	ZVN1404A	6
ZVN0102A	2	ZVN1406A	6
ZVN0102B	2	ZVN1408A	6
ZVN0102L	2	ZVN1409A	6
ZVN0106A	2	ZVN2104A	2
ZVN0106B	2	ZVN2104B	2
ZVN0106L	2	ZVN2104L	2
ZVN0108A	2	ZVN2106A	2
ZVN0108B	2	ZVN2106B	2
ZVN0108L	2	ZVN2106L	2
ZVN0117TA	2	ZVN2110A	2
ZVN0120A	2	ZVN2110B	2
ZVN0120B	2	ZVN2110L	2
ZVN0120L	2	ZVN2115A	2
ZVN0526A	4	ZVN2115B	2
ZVN0530A	4	ZVN2115L	2
ZVN0530B	4	ZVN2202B	3
ZVN0530L	4	ZVN2202L	3
ZVN0535A	4	ZVN2204B	3
ZVN0535B	4	ZVN2204L	3
ZVN0535L	4	ZVN2206B	3
ZVN1306A	5	ZVN2206L	3
ZVN1306B	5	ZVN2208B	3
		ZVN2208L	3

ALPHA-NUMERIC PRODUCT LIST

DEVICE	DATA SECTION
ZVN2210B	3
ZVN2210L	3
ZVN2215B	3
ZVN2215L	3
ZVN2220B	3
ZVN2220L	3
ZVN2224B	3
ZVN2224L	3
ZVN3302A	5
ZVN3302B	5
ZVN3304A	5
ZVN3304B	5
ZVN3306A	5
ZVN3306B	5
ZVN3310A	5
ZVN3310B	5
ZVN3315A	5
ZVN3315B	5
ZVP0102A	REFER
ZVP0102B	"
ZVP0102L	"
ZVP0106A	"
ZVP0106B	"
ZVP0106L	"
ZVP0108A	"
ZVP0108B	"
ZVP0108L	"
ZVP0120A	REFER
ZVP0120B	"
ZVP0120L	"
ZVP0530A	"
ZVP0530B	"
ZVP0530L	"
ZVP0535A	"
ZVP0535B	"
ZVP0535L	"
ZVP1306A	"
ZVP1306B	"
ZVP1308A	"
ZVP1308B	"
ZVP1320A	"
ZVP1320B	"
ZVP2104A	"
ZVP2104B	"
ZVP2104L	"
ZVP2106A	"
ZVP2106B	"
ZVP2106L	"
ZVP2110A	"
ZVP2110B	"
ZVP2110L	"
ZVP2115A	"
ZVP2115B	"
ZVP2115L	"
ZVP2202B	"
ZVP2202L	"

ALPHA-NUMERIC PRODUCT LIST

DEVICE	DATA SECTION	DEVICE	DATA SECTION
ZVP2204B	REFER	ZVP3302A	REFER
ZVP2204L	"	ZVP3302B	"
ZVP2206B	"	ZVP3304A	"
ZVP2206L	"	ZVP3304B	"
ZVP2208B	"	ZVP3306A	"
ZVP2208L	"	ZVP3306B	"
ZVP2210B	"	ZVP3310A	"
ZVP2210L	"	ZVP3310B	"
ZVP2215B	"	ZVP3315A	"
ZVP2215L	"	ZVP3315B	"
ZVP2220B	"		
ZVP2220L	"		

MOSFETS TO BS-CECC

CECC NUMBER	COMMERCIAL EQUIVALENT	APPROVAL STATUS
50012-018	ZVN2104A ZVN2106A ZVN0108A ZVN2110A	C
50012-019	ZVN0530A ZVN0535A	C
50012-020	ZVN2115L ZVN0120L	C
50012-031	ZVN2104B ZVN2106B ZVN0108B ZVN2110B	C
50012-032	ZVN2204B ZVN2206B ZVN2208B ZVN2210B	P
50012-033	ZVP2104A ZVP2106A ZVP0108A ZVP2110A	P
50012-034	ZVP2104B ZVP2106B ZVP0108B ZVP2110B	P
50012-035	ZVP2204B ZVP2206B ZVP2208B ZVP2210B	P

C = Current P = Pending

MOSFETS TO BS-CECC

FERRANTI TYPE	BS-CECC NUMBER	APPROVAL STATUS
ZVN0108A	50012-018	C
ZVN0108B	50012-031	C
ZVN0120L	50012-020	C
ZVN0530A	50012-019	C
ZVN0535A	50012-019	C
ZVN2104A	50012-018	C
ZVN2104B	50012-031	C
ZVN2106A	50012-018	C
ZVN2106B	50012-031	C
ZVN2110A	50012-018	C
ZVN2110B	50012-031	C
ZVN2115L	50012-020	C
ZVN2204B	50012-032	P
ZVN2206B	50012-032	P
ZVN2208B	50012-032	P
ZVN2210B	50012-032	P
ZVP0108A	50012-033	P
ZVP0108B	50012-034	P
ZVP2104A	50012-033	P
ZVP2104B	50012-034	P
ZVP2106A	50012-033	P
ZVP2106B	50012-034	P
ZVP2110A	50012-033	P
ZVP2110B	50012-034	P
ZVP2204B	50012-035	P
ZVP2206B	50012-035	P
ZVP2208B	50012-035	P
ZVP2210B	50012-035	P

N-CHANNEL DEVICES

N-CHANNEL MOSFET SELECTION GUIDE

BV_{DSS} V Min.	$R_{DS(ON)}$ Ω Max.	@ I_D A	Device	$I_{D(cont)}$ A Max.	P_D W	Package
350	50	0.1	ZVN0535A	0.09	0.7	E-Line
			ZVN0535B	0.15	5	TO-39
			ZVN0535L	0.15	20	TO-220
300			ZVN0530A	0.09	0.7	E-Line
			ZVN0530B	0.15	5	TO-39
			ZVN0530L	0.15	20	TO-220
260	40		ZVN0526A	0.10	0.7	E-Line
240	6	0.5	ZVN2224B	1.20	20	TO-39
			ZVN2224L	1.20	20	TO-220
200	40	0.1	ZVN1320A	0.10	0.625	E-Line
			ZVN1320B	0.25	5	TO-39
	28	0.020	BS107PT	0.12	0.5	E-Line
	23	0.025	BS107P	0.12	0.5	E-Line
	16	0.25	ZVN0120A	0.16	0.7	E-Line
			ZVN0120B	0.42	5	TO-39
			ZVN0120L	0.50	20	TO-220
	2.5	1.0	ZVN2220B	1.85	20	TO-39
			ZVN2220L	1.85	20	TO-220
170	23	0.1	ZVN0117TA	0.1	0.7	E-Line
150	40		ZVN3315A	0.1	0.625	E-Line
			ZVN3315B	0.25	5	TO-39
	16	0.25	ZVN2115A	0.16	0.7	E-Line
			ZVN2115B	0.42	5	TO-39
			ZVN2115L	0.50	20	TO-220
	2.5	1.0	ZVN2215B	1.85	20	TO-39
			ZVN2215L	1.85	20	TO-220
100	10	0.50	ZVN3310A	0.2	0.625	E-Line
			ZVN3310B	0.5	5	TO-39
	4	1.0	ZVN2110A	0.32	0.7	E-Line
			ZVN2110B	0.85	5	TO-39
			ZVN2110L	1.560	20	TO-220
	0.8	2.0	ZVN2210B	3.45	20	TO-39
			ZVN2210L	3.45	20	TO-220

N-CHANNEL MOSFET SELECTION GUIDE

BV_{DSS} V Min.	$R_{DS(ON)}$ Ω Max.	@ I_D A	Device	$I_{D(cont)}$ A Max.	P_D W	Package
90	250	0.005	ZVN1409A	0.01	0.625	E-Line
80			ZVN1408A	0.01	0.625	E-Line
	10	0.5	ZVN1308A	0.2	0.625	E-Line
			ZVN1308B	0.5	5	TO-39
	4	1.0	ZVN0108A	0.32	0.7	E-Line
			ZVN0108B	0.85	5	TO-39
			ZVN0108L	1.5	20	TO-220
60	250	0.005	ZVN1406A	0.01	0.625	E-Line
	10	0.50	ZVN1306A	0.2	0.625	E-Line
			ZVN1306B	0.5	5	TO-39
	5	0.50	VN10LP	0.3	0.625	E-Line
			ZVN3306A	0.27	0.625	E-Line
			ZVN3306B	0.75	5	TO-39
		0.2	BS170P	0.5	0.625	E-Line
	4	1.0	ZVN0106A	0.32	0.7	E-Line
			ZVN0106B	0.85	5	TO-39
			ZVN0106L	1.5	20	TO-220
	2		ZVN2106A	0.45	0.7	E-Line
			ZVN2106B	1.2	5	TO-39
			ZVN2106L	2.0	20	TO-220
	0.5	2.0	ZVN2206B	4.8	20	TO-39
			ZVN2206L	4.8	20	TO-220
40	250	0.006	ZVN1404A	0.01	0.625	E-Line
	5	0.5	ZVN3304A	0.27	0.625	E-Line
			ZVN3304B	0.75	5	TO-39
	2	1.0	ZVN2104A	0.45	0.7	E-Line
			ZVN2104B	1.2	5	TO-39
			ZVN2104L	2.0	20	TO-220
	0.5	2.0	ZVN2204B	4.8	20	TO-39
			ZVN2204L	4.8	20	TO-220
20	5	0.5	ZVN3302A	0.27	0.625	E-Line
			ZVN3302B	0.75	5	TO-39

N-CHANNEL MOSFET SELECTION GUIDE

BV_{DSS} V Min.	$R_{DS(ON)}$ Ω Max. @	I_D A	Device	$I_{D(cont)}$ A Max.	P_D W	Package
20	2	1.0	ZVN0102A	0.45	0.7	E-Line
			ZVN0102B	1.2	5	TO-39
			ZVN0102L	2.0	20	TO-220
	0.5	2.0	ZVN2202B	4.8	20	TO-39
			ZVN2202L	4.8	20	TO-220

NOTES

NOTES

DATA INDEX

SECTION	RANGE	DEVICES
1	Industry Standard	BS107P BS107PT BS170P VN10LP
2	ZVN21	ZVN2106A/B/L ZVN2110A/B/L ZVN0117TA ZVN0120A/B/L
3	ZVN22	ZVN2206B/L ZVN2210B/L ZVN2220B/L ZVN2224B/L
4	ZVN05	ZVN0526A ZVN0535A/B/L
5	ZVN33	ZVN3306A/B ZVN3310A/B ZVN1320A/B
6	ZVN14	ZVN1409A

NOTES

NOTES

Section 1

Industry Standards

BS107P

BS107PT

BS170P

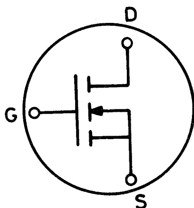
VN10LP

FERRANTI semiconductors®

BS107P

N-Channel Enhancement-Mode Vertical DMOS Power FET

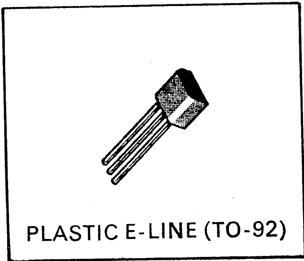
200V: 23 ohm: 120mA



N-Channel

FEATURES

- High Breakdown Voltage
- High Input Impedance
- High Speed Switching
- No Minority Storage Time
- CMOS Logic Compatible Input
- Low Current Drive
- No Secondary Breakdown
- Excellent Temperature Stability
- Specially Suited for Telephone Subsets



PLASTIC E-LINE (TO-92)

DESCRIPTION

Compact geometries are the basis of the new generation of FERRANTI Power MOSFET transistors, optimised for low ON-resistance, low capacitances and fast switching speeds.

This particular device is specially designed for use in telephone switching circuits.

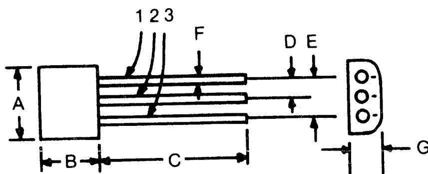
It is capable of withstanding simulated surges of lightning, to the circuit, of up to 1.5KV as laid down by British Telecom.

PRODUCT SUMMARY

BV_{DSS} 200V
$I_{D(CONT)}$ 120mA
$R_{DS(ON)}$ 23Ω
P_D 500mW

Chip Size 0.042″ × 0.042″

PACKAGE DIMENSIONS



PIN OUT	
1	Drain
2	Gate
3	Source

Also available with various lead bends and on Tape and Reel.

SYMBOL	INCHES		MILLIMETRES	
	MIN	MAX	MIN	MAX
A	.172	.188	4.37	4.77
B	.142	.158	3.61	4.01
C	.475	.525	12.06	13.34
D	.05		1.27	
E	.10		2.54	
F	.016	.019	.406	.495
G	.085	.095	2.16	2.42

BS107P

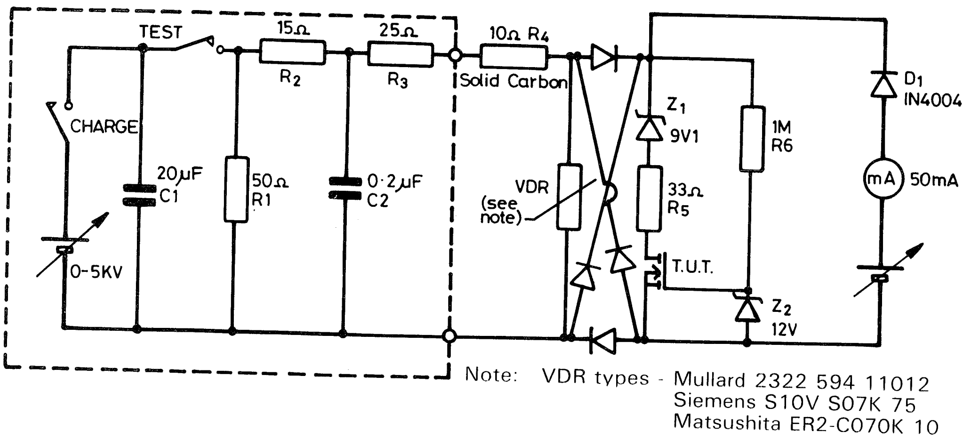
ABSOLUTE MAXIMUM RATINGS

Parameters	Symbol	Value	Units
Drain-source voltage	BV_{DSS}	200	V
Continuous drain current (@ $T_A = 25°C$)	I_D	120	mA
Pulse drain current	I_{DM}	2	A
Gate-source voltage	V_{GS}	±20	V
Power dissipation (@ $T_A = 25°C$)	P_D	0.5	W
Operating/Storage Temperature Range	T_j, T_{stg}	−55 to +150	°C

ELECTRICAL CHARACTERISTICS (at T = 25°C unless otherwise stated)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Drain-source breakdown voltage	BV_{DSS}	200	230	-	V	$I_D = 100\mu A$, $V_{GS} = 0$
Gate-body leakage current	I_{GSS}	-	-	10	nA	$V_{GS} = 15V$, $V_{DS} = 0$
Drain cut-off current	I_{DSS}	-	-	30	nA	$V_{DS} = 130V$, $V_{GS} = 0$
	I_{DSX}	-	-	1	μA	$V_{DS} = 70V$, $V_{GS} = 0.2V$
Drain-source ON-resistance	$R_{DS(ON)}$	-	15	23	Ω	$V_{GS} = 2.6V$, $I_D = 25mA$
		-	-	30	Ω	$V_{GS} = 5V$, $I_D = 100mA$

SURGE TEST CIRCUIT FOR OUTPULSING FET



Note: VDR types - Mullard 2322 594 11012
Siemens S10V S07K 75
Matsushita ER2-C070K 10

6872

The transistor under test should withstand a surge applied via above circuit when C1 is charged to 1.5kV.

Fig. 1 Output Characteristics

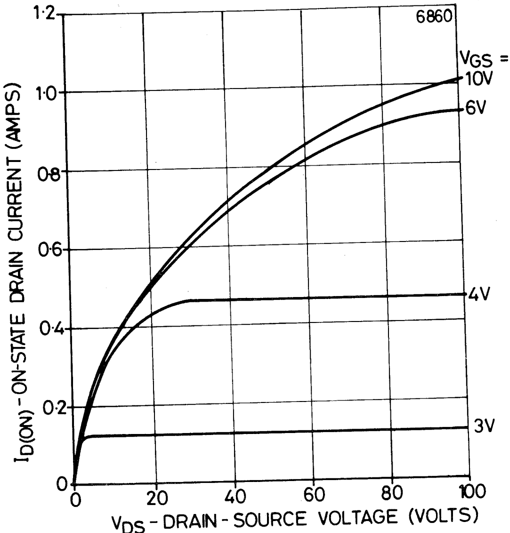
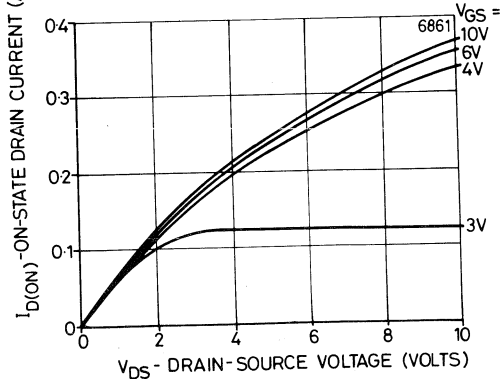


Fig. 2 Saturation Characteristics



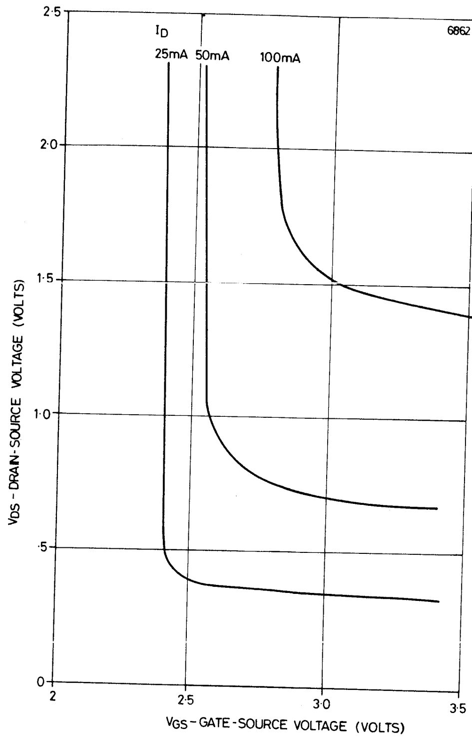


Fig. 3 Voltage Saturation Characteristics

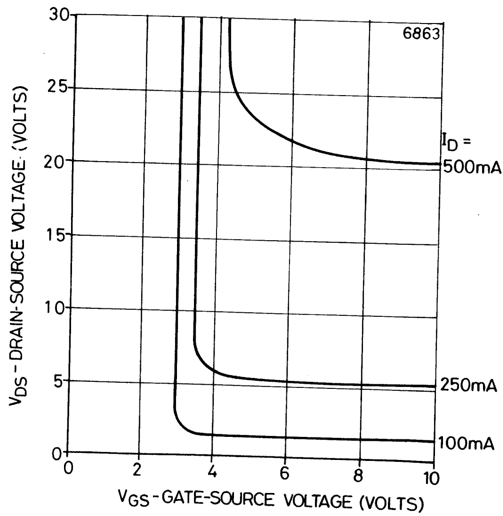


Fig. 4 Voltage Saturation Characteristics

Fig. 5 Transfer Characteristics

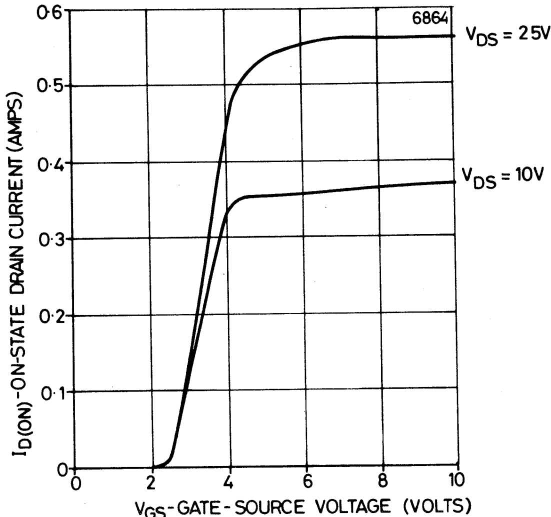


Fig. 6 Capacitance vs Drain-Source Voltage

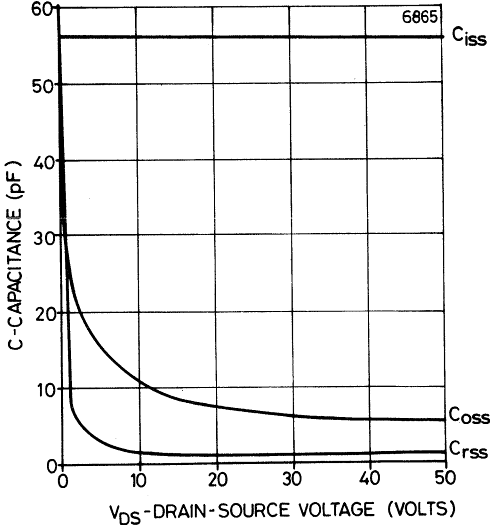


Fig. 7 Transconductance vs Drain-Current

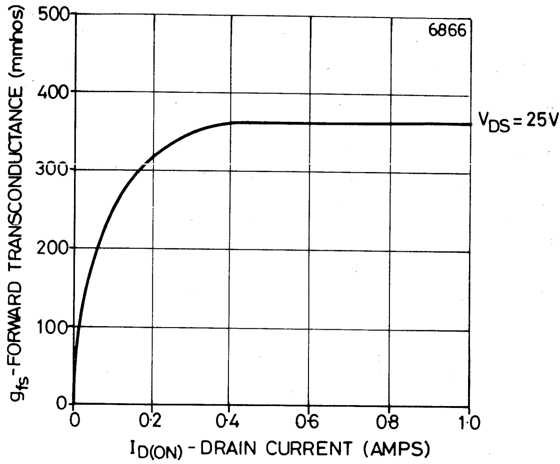


Fig. 8 Transconductance vs Gate-Source Voltage

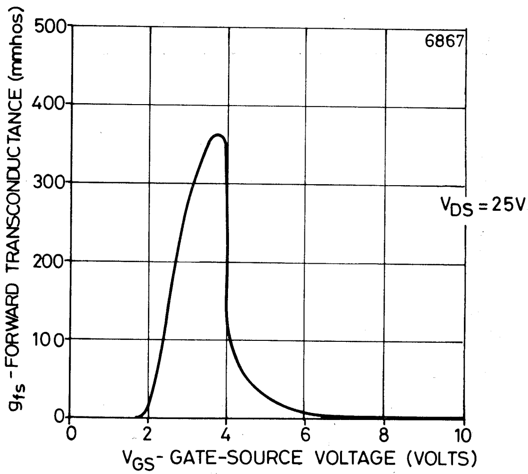


Fig. 9 Gate Charge vs Gate-Source Voltage

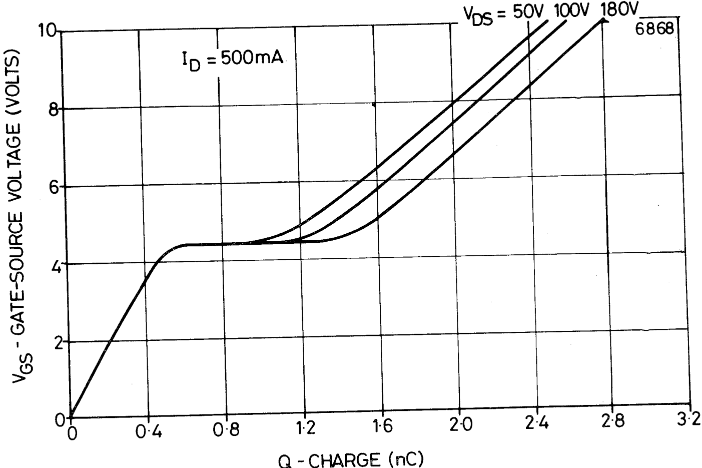
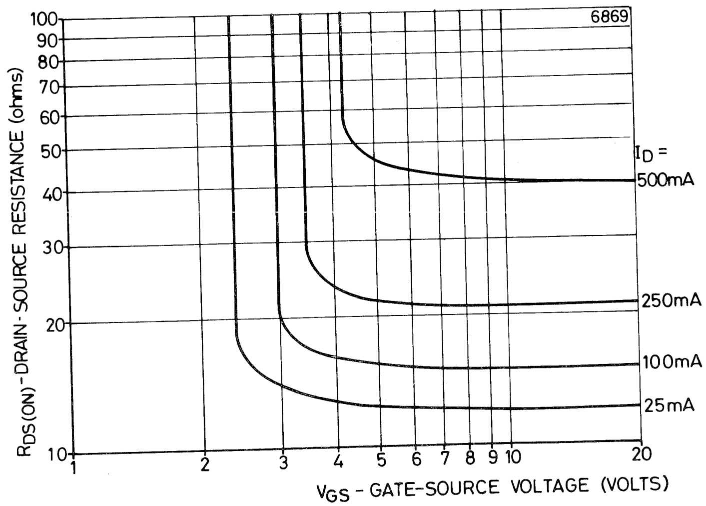


Fig. 10 ON-Resistance vs Gate-Source Voltage



BS107P

Fig. 11 Variation of $R_{DS(ON)}$ and $V_{GS(th)}$ with Temperature

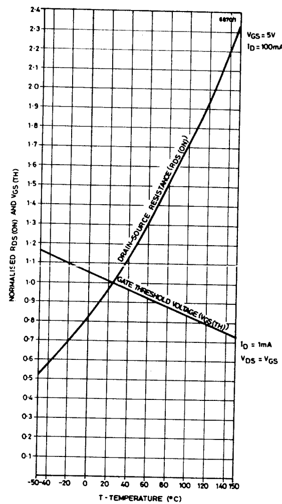
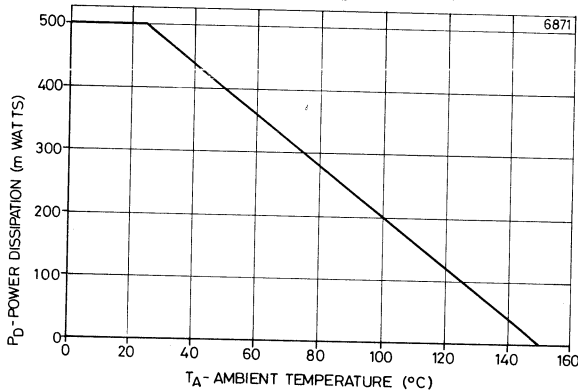


Fig. 12 Power Derating (Ambient)



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Issue 2, April 1984 4.5M

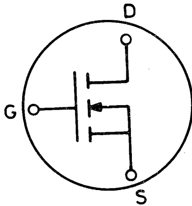
Printed in England CP

FERRANTI semiconductors®

BS107PT

N-Channel Enhancement-Mode Vertical DMOS Power FET

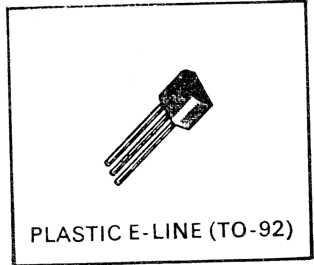
200V: 28 ohm: 120mA



N-Channel

FEATURES

- High Breakdown Voltage
- High Input Impedance
- High Speed Switching
- No Minority Storage Time
- CMOS Logic Compatible Input
- Low Current Drive
- No Secondary Breakdown
- Excellent Temperature Stability
- Specially Suited for Telephone Subsets



PLASTIC E-LINE (TO-92)

DESCRIPTION

Compact geometries are the basis of the new generation of FERRANTI Power MOSFET transistors, optimised for low ON-resistance, low capacitances and fast switching speeds.

This particular device is specially designed for use in telephone switching circuits.

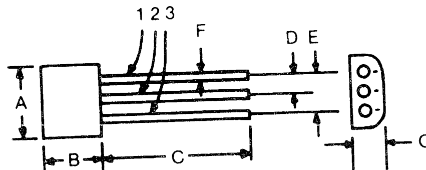
It is capable of withstanding simulated surges of lightning, to the circuit, of up to 1.5KV as laid down by British Telecom.

PRODUCT SUMMARY

BV_{DSS} 200V
$I_{D(CONT)}$ 120mA
$R_{DS(ON)}$ 28Ω
P_D 500mW

Chip Size 0.042″ × 0.042″

PACKAGE DIMENSIONS



PIN OUT	
1	Drain
2	Gate
3	Source

SYMBOL	INCHES		MILLIMETRES	
	MIN	MAX	MIN	MAX
A	.172	.188	4.37	4.77
B	.142	.158	3.61	4.01
C	.475	.525	12.06	13.34
D	.05		1.27	
E	.10		2.54	
F	.016	.019	.406	.495
G	.085	.095	2.16	2.42

Also available with various lead bends and on Tape and Reel.

BS107PT

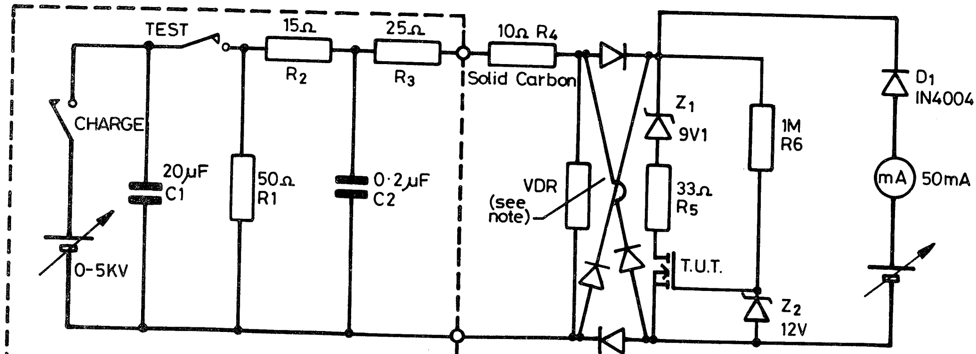
ABSOLUTE MAXIMUM RATINGS

Parameters	Symbol	Value	Units
Drain-source voltage	BV_{DSS}	200	V
Continuous drain current (@ $T_A = 25°C$)	I_D	120	mA
Pulse drain current	I_{DM}	2	A
Gate-source voltage	V_{GS}	±20	V
Power dissipation (@ $T_A = 25°C$)	P_D	0.5	W
Operating/Storage Temperature Range	T_j, T_{stg}	−55 to +150	°C

ELECTRICAL CHARACTERISTICS (at T = 25°C unless otherwise stated)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Drain-source breakdown voltage	BV_{DSS}	200	230	-	V	$I_D = 100\mu A$, $V_{GS} = 0$
Gate-body leakage current	I_{GSS}	-	-	10	nA	$V_{GS} = 15V$, $V_{DS} = 0$
Drain cut-off current	I_{DSS}	-	-	30	nA	$V_{DS} = 130V$, $V_{GS} = 0$
	I_{DSX}	-	-	1	μA	$V_{DS} = 70V$, $V_{GS} = 0.2V$
Drain-source ON-resistance	$R_{DS(ON)}$	-	15	28	Ω	$V_{GS} = 2.6V$, $I_D = 20mA$
		-	-	30	Ω	$V_{GS} = 2.7V$, $I_D = 100mA$

SURGE TEST CIRCUIT FOR OUTPULSING FET



Note: VDR types - Mullard 2322 594 11012
Siemens S10V S07K 75
Matsushita ER2-C070K 10

6872

The transistor under test should withstand a surge applied via above circuit when C1 is charged to 1.5kV.

Fig. 1 Output Characteristics

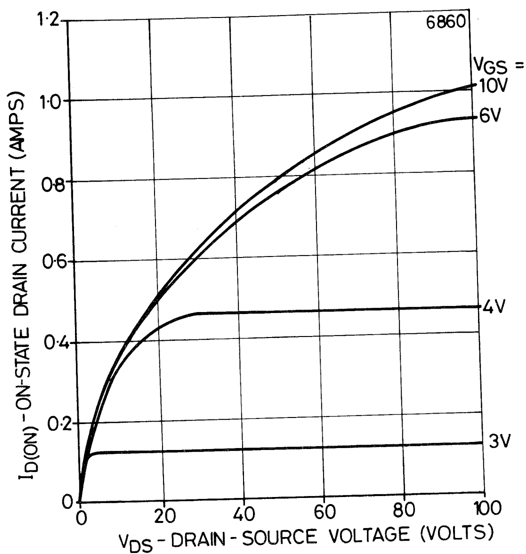


Fig. 2 Saturation Characteristics

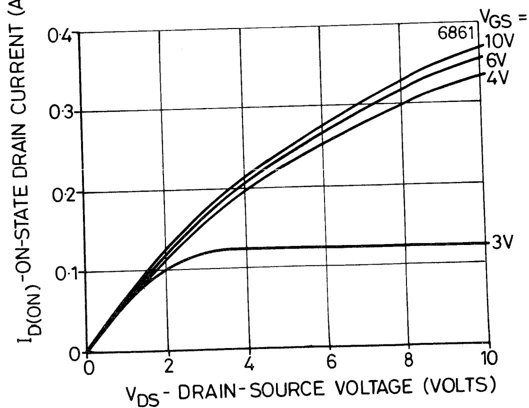


Fig. 3 Voltage Saturation Characteristics

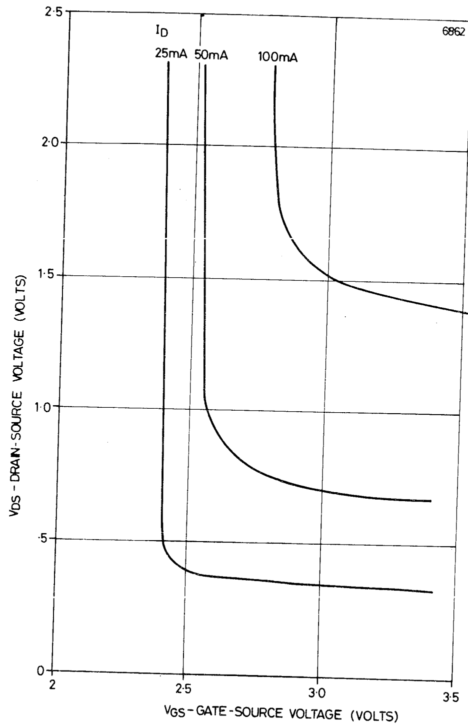


Fig. 4 Voltage Saturation Characteristics

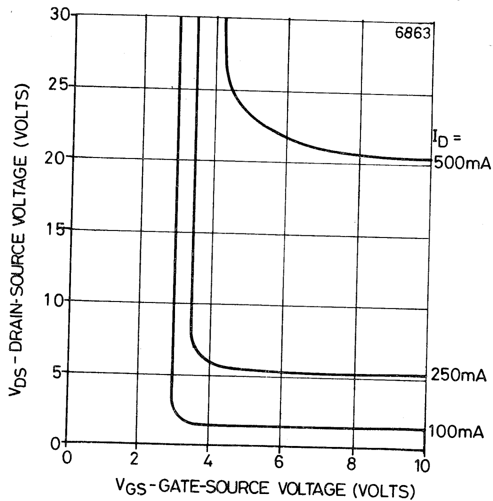


Fig. 5 Transfer Characteristics

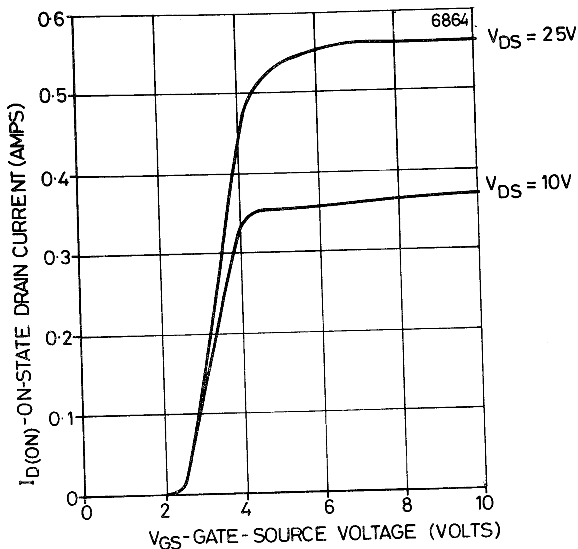


Fig. 6 Capacitance vs Drain-Source Voltage

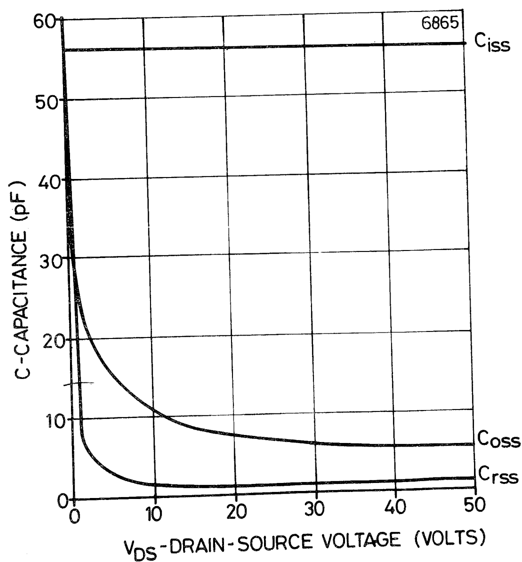


Fig. 7 Transconductance vs Drain-Current

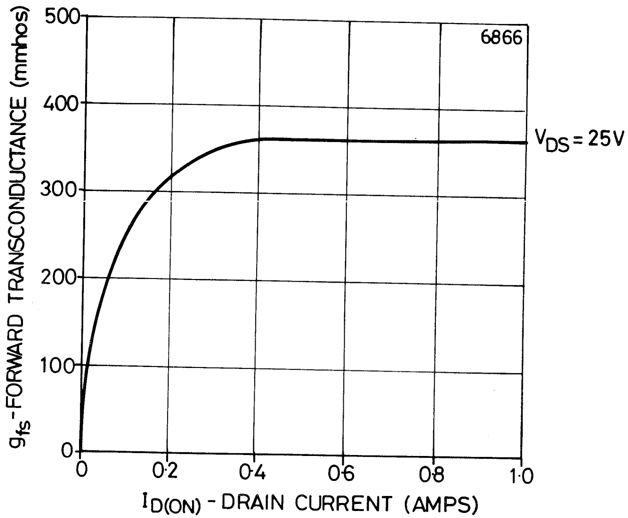


Fig. 8 Transconductance vs Gate-Source Voltage

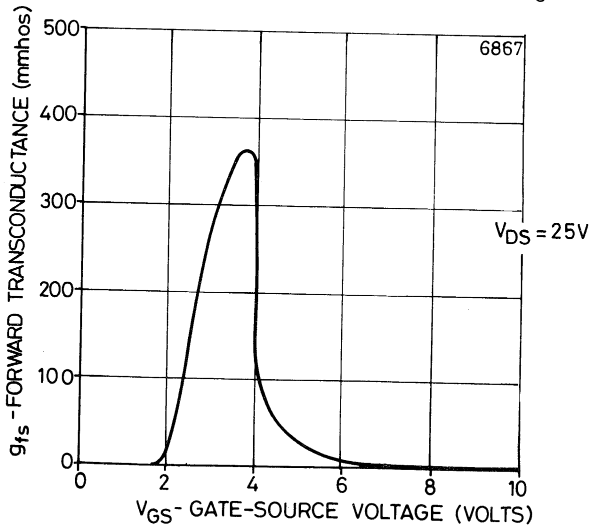


Fig. 9 Gate Charge vs Gate-Source Voltage

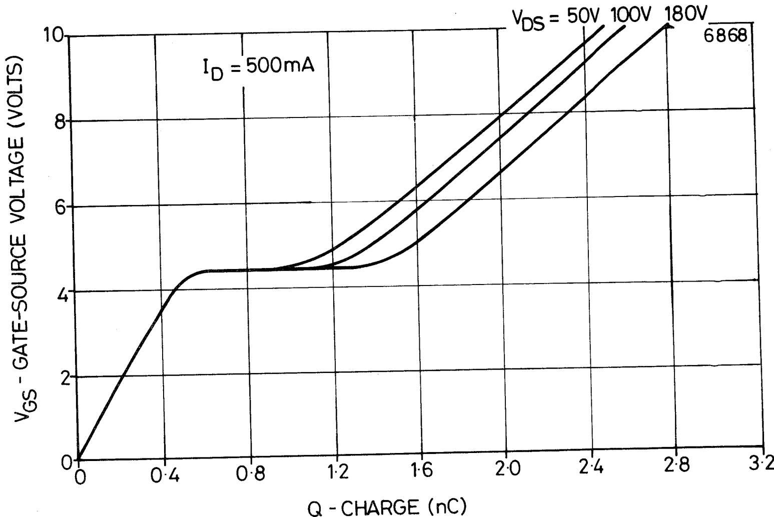
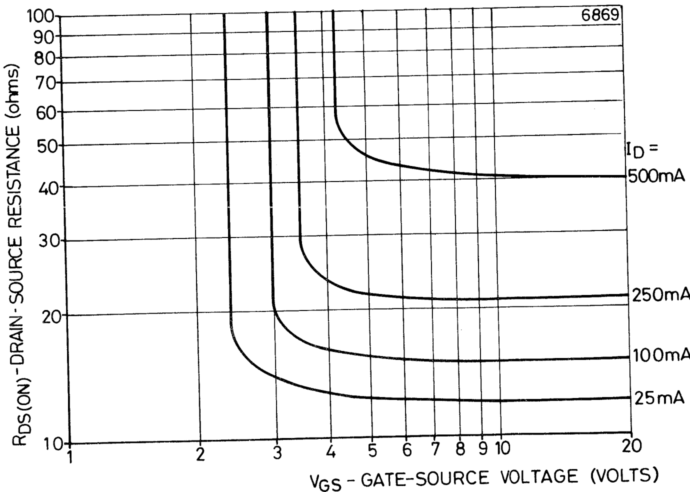


Fig. 10 ON-Resistance vs Gate-Source Voltage



BS107PT

Fig. 11 Variation of $R_{DS(ON)}$ and $V_{GS(th)}$ with Temperature

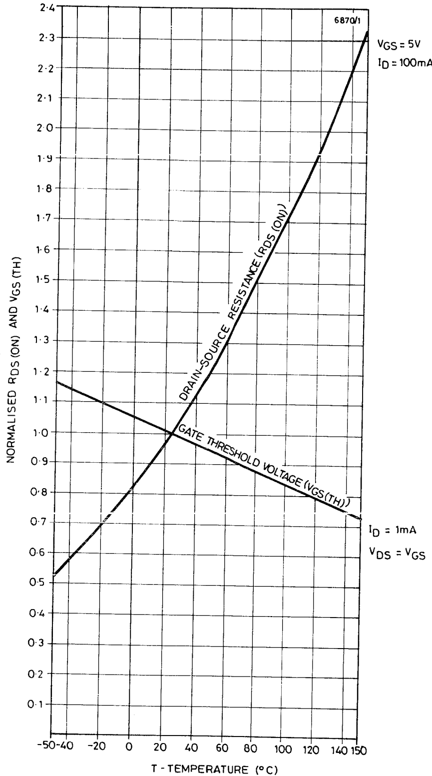
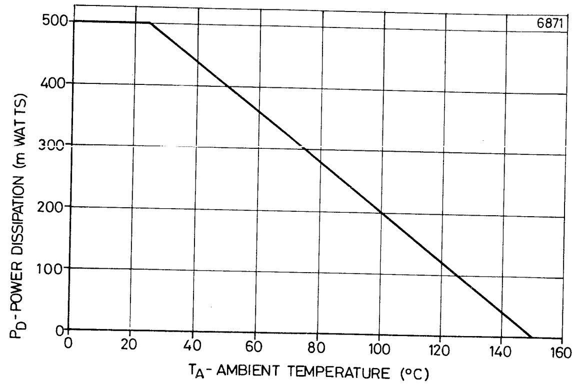


Fig. 12 Power Derating (Ambient)



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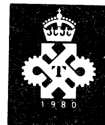
Ferranti Wheelock Microelectronics Limited, 65 Wong Chuk Hang Road, 17/F., Flat D,
Gee Chang Hong Centre, Aberdeen, Hong Kong Tel: 5-538298-9 Telex: HX 74605



Issue 1, May 1984 4.5M

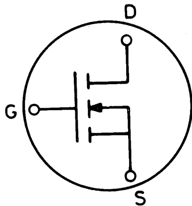
Printed in England CP

FERRANTI semiconductors®

BS170P

N-Channel Enhancement-Mode Vertical DMOS Power FET

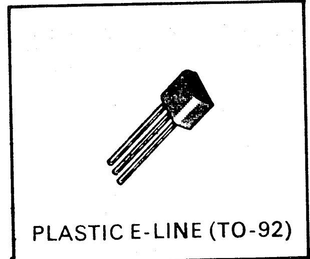
60V: 5 ohm: 0.5A



N-Channel

FEATURES

- Fast Switching Speeds
- No Secondary Breakdown
- Excellent Temperature Stability
- High Input Impedance
- Low Current Drive



PLASTIC E-LINE (TO-92)

DESCRIPTION

Compact OVERLAY (CELL) and INTER-DIGITATED geometries are the basis of the new generation of FERRANTI Power MOSFET transistors. These efficient geometries, optimised for low ON-resistance, low capacitances and fast switching speeds, with computer controlled processing combine to achieve greater device ruggedness.

The planar construction, coupled with ion implantation and the self-aligned poly-silicon gate manufacturing process, provides the reliability and stability in performance required in todays designs.

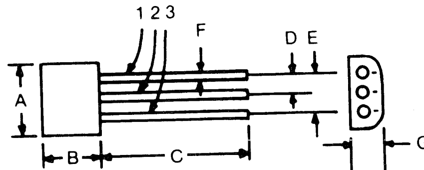
PRODUCT SUMMARY

Device Type	BV_{DSS}	$I_{D(CONT)}$	$R_{D(ON)}$
BS170P	60V	0.5A	5Ω

Chip Size 0.030" × 0.030" (ZVN13/33)

FERRANTI Power MOSFETS will directly interface with MICROPROCESSORS, LOGIC ARRAYS and standard IC LOGIC families including CMOS, TTL, PMOS and NMOS.

PACKAGE DIMENSIONS



PIN OUT	
1	Drain
2	Gate
3	Source

Also available with various lead bends and on Tape and Reel.

SYMBOL	INCHES		MILLIMETRES	
	MIN	MAX	MIN	MAX
A	.172	.188	4.37	4.77
B	.142	.158	3.61	4.01
C	.475	.525	12.06	13.34
D	.05		1.27	
E	.10		2.54	
F	.016	.019	.406	.495
G	.085	.095	2.16	2.42

ABSOLUTE MAXIMUM RATINGS

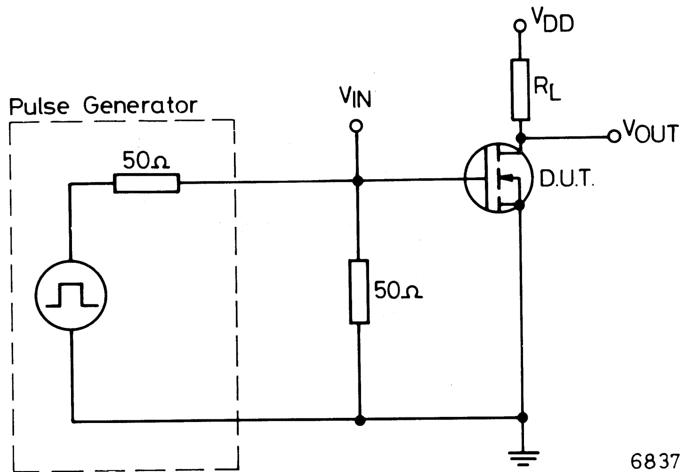
Parameters	Symbol	Value	Units
Drain-source voltage	V_{DS}	60	V
Continuous drain current (@ $T_A = 25°C$) (@ $T_C = 25°C$)	I_D I_D	0.27 -	A A
Pulse drain current	I_{DM}	3	A
Gate-source voltage	V_{GS}	±20	V
Power dissipation (@ $T_A = 25°C$) (@$T_C = 25°C$)	P_D	0.625 -	W W
Operating/Storage Temperature Range		−55 to +150	°C

ELECTRICAL CHARACTERISTICS (at T = 25°C unless otherwise stated)

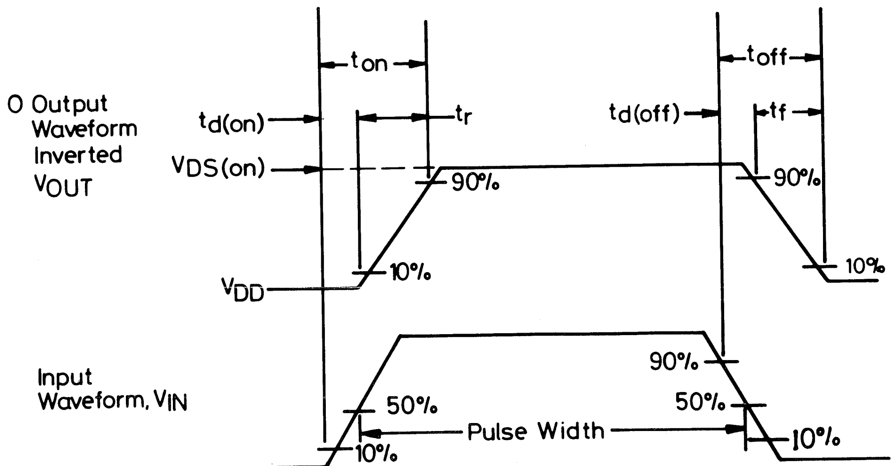
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Drain-source breakdown voltage	BV_{DSS}	60	90	-	V	$I_D = 100\mu A$, $V_{GS} = 0$
Gate-source threshold voltage	$V_{GS(th)}$	0.8	-	3	V	$I_D = 1mA$, $V_{DS} = V_{GS}$
Gate-body leakage	I_{GSS}	-	-	10	nA	$V_{GS} = 15V$, $V_{DS} = 0$
Drain cut-off current (Note 2)	$I_{D(off)}$	-	-	0.5	μA	$V_{DS} = 25V$, $V_{GS} = 0$
Static drain-source ON-resistance*	$R_{DS(ON)}$	-	3.5	5	Ω	$I_D = 0.2A$, $V_{GS} = 10V$
Forward transconductance* (Note 2)	g_{fs}	-	200	-	mS	$V_{DS} = 10V$, $I_D = 0.2A$
Input capacitance (Note 2)	C_{iss}	-	60	-	pF	$V_{DS} = 10V$, $V_{GS} = 0$ f = 1MHz
Turn-on time (Notes 1 & 2)	$t_{d(on)}$	-	-	10	n secs	$I_D = 0.2A$
Turn-off time (Notes 1 & 2)	$t_{d(off)}$	-	-	10	n secs	$I_D = 0.2A$

*Measured under pulsed conditions. Width = 300μS. Duty cycle ⩽ 2%.
Note 1 Switching times measured with 50ohm source impedance and <5ns rise time.
Note 2 Sample test.

Circuit for Measuring Switching Times



Switching Waveforms



Note:
Power MOSFET switching times are essentially independent of operating temperature

Fig. 1 Saturation Characteristics

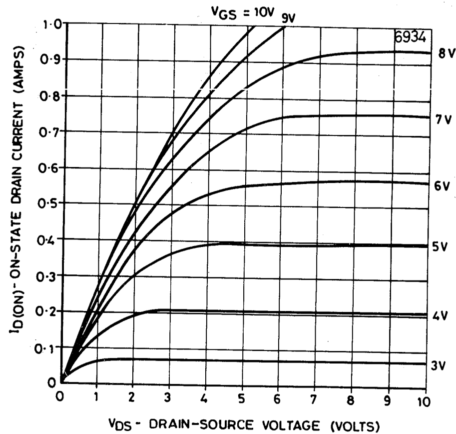


Fig. 2 Voltage Saturation Characteristics

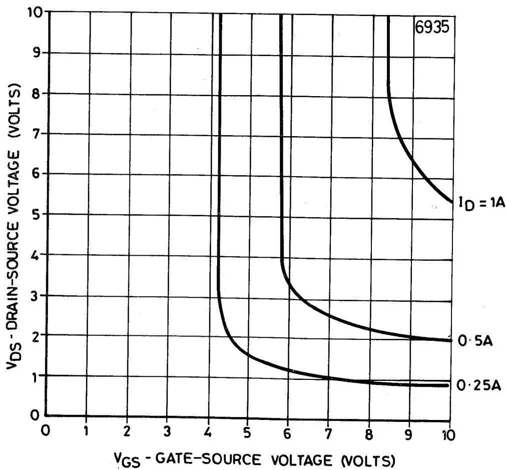


Fig. 3 Transfer Characteristics

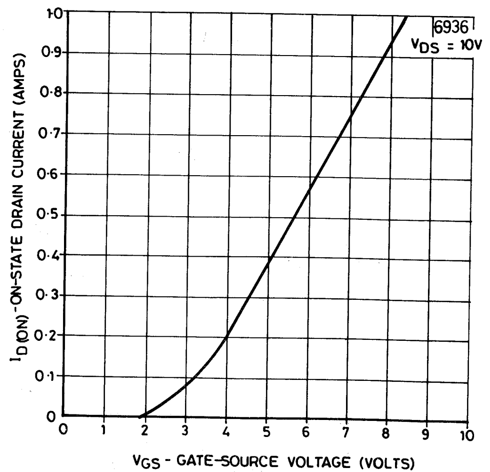


Fig. 4 Capacitance vs Drain-Source Voltage

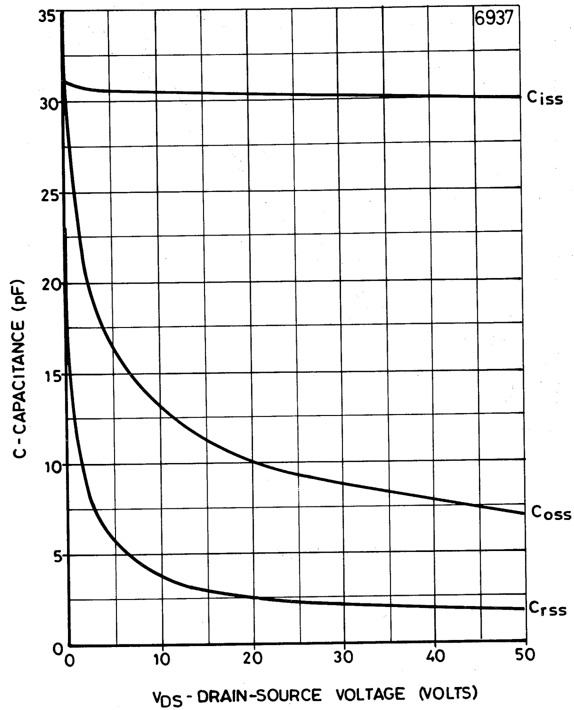


Fig. 5 Transconductance vs Drain-Current

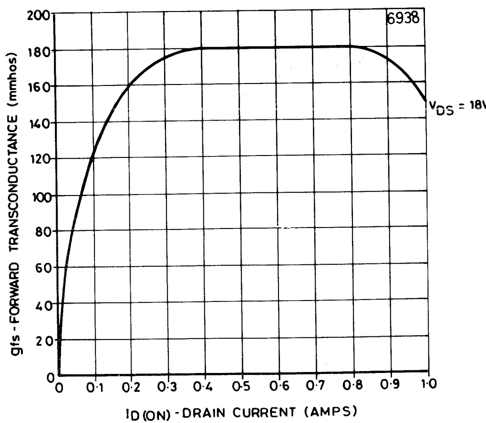


Fig. 6 Transconductance vs Gate-Source Voltage

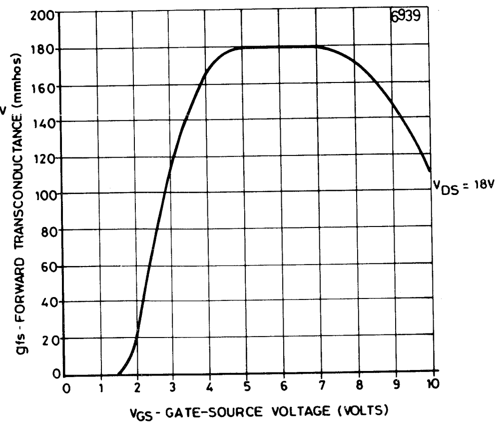


Fig. 7 Gate Charge vs Gate-Source Voltage

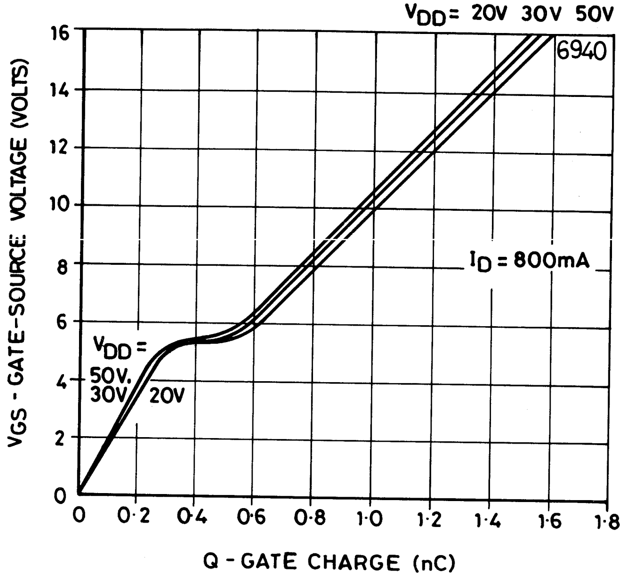


Fig. 8 ON-Resistance vs Gate-Source Voltage

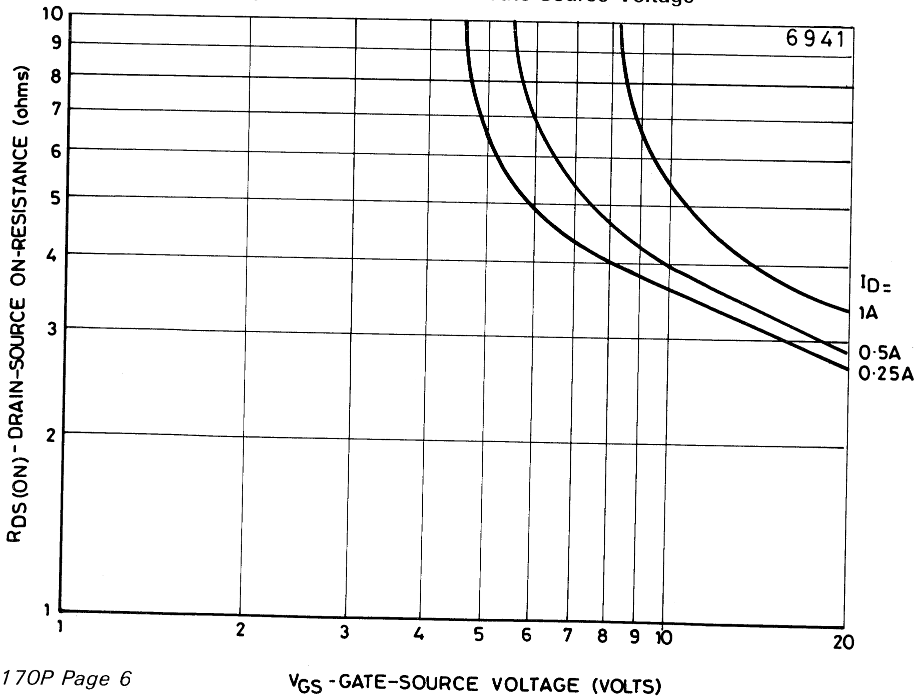


Fig. 9 Variation of $R_{DS(ON)}$ and $V_{GS(th)}$ with Temperature

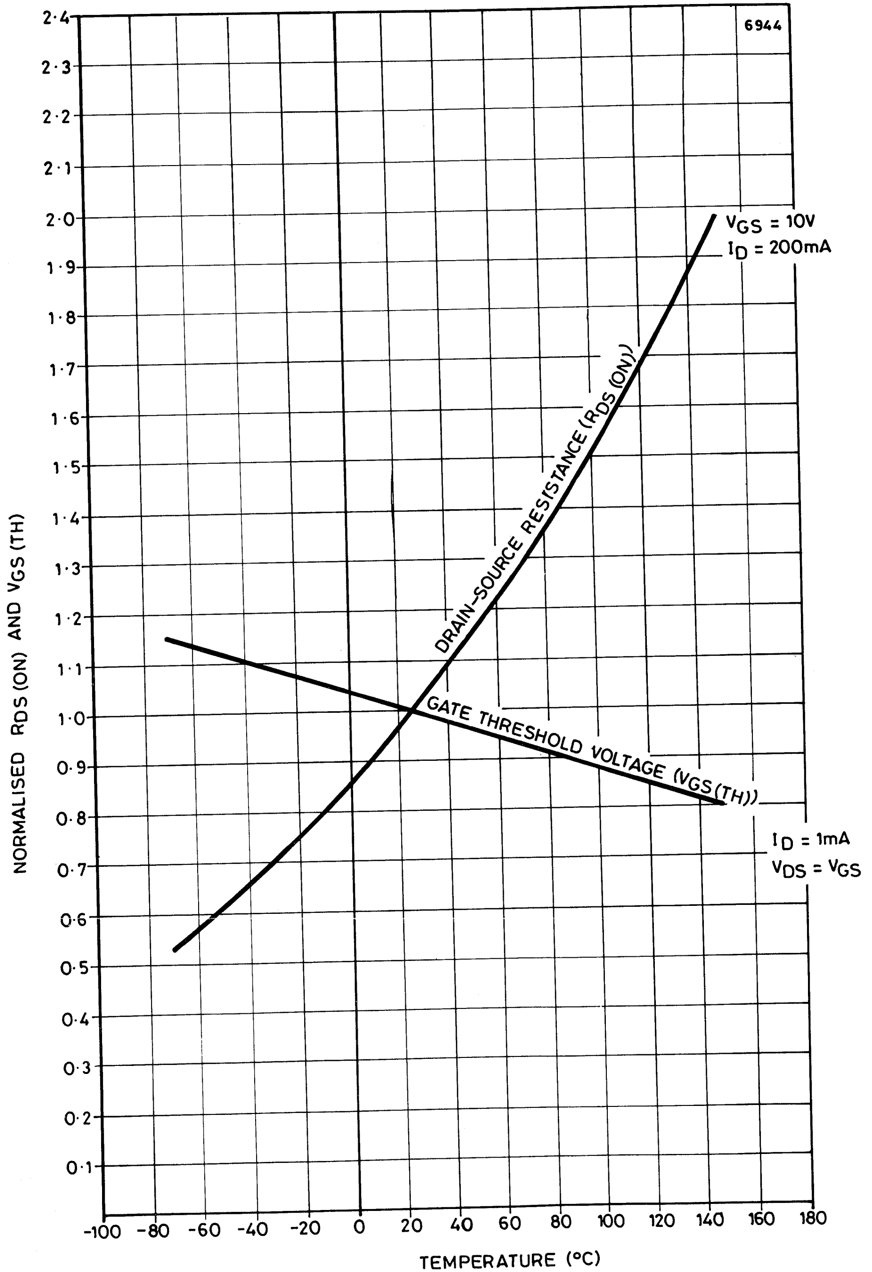
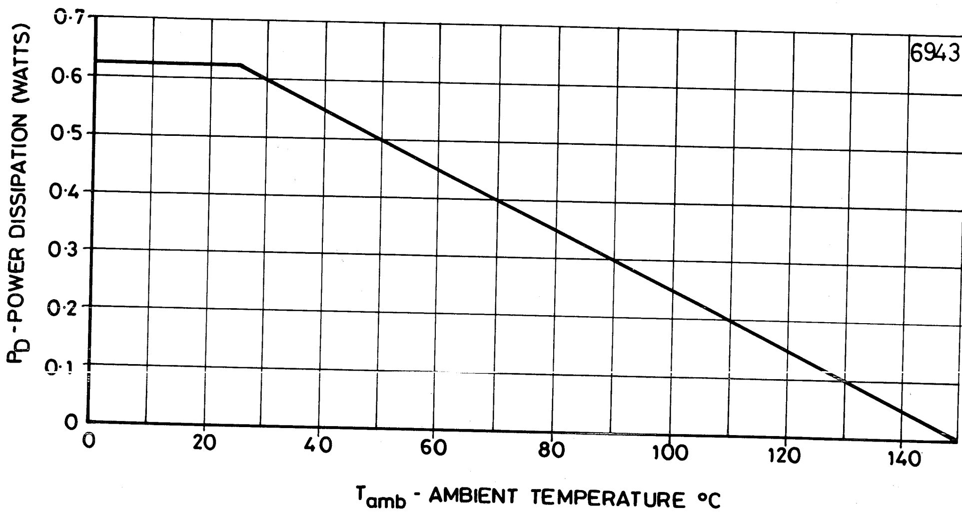


Fig. 10 Power Derating (Ambient)



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Issue 1, May 1984 4.5M

Printed in England CP

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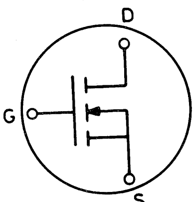
VN10LP

N-Channel Enhancement-Mode Vertical DMOS Power FET

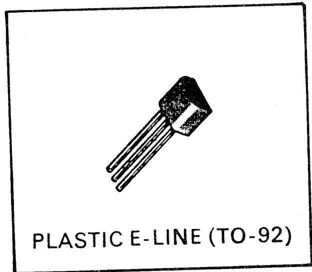
60V: 5 ohm: 0.3A



N-Channel

FEATURES

- Compact Geometry
- Fast Switching Speeds
- No Secondary Breakdown
- Excellent Temperature Stability
- High Input Impedance
- Low Current Drive
- Ease of Paralleling



PLASTIC E-LINE (TO-92)

DESCRIPTION

Compact OVERLAY (CELL) and INTER-DIGITATED geometries are the basis of the new generation of FERRANTI Power MOSFET transistors. These efficient geometries, optimised for low ON-resistance, low capacitances and fast switching speeds, with computer controlled processing combine to achieve greater device ruggedness.

The planar construction, coupled with ion implantation and the self-aligned poly-silicon gate manufacturing process, provides the reliability and stability in performance required in todays designs.

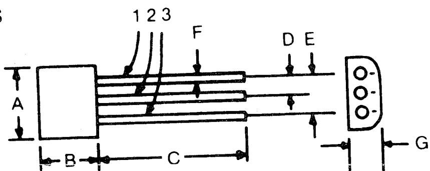
PRODUCT SUMMARY

Device Type	BV_{DSS}	$I_{D(CONT)}$	$R_{D(ON)}$
VN10LP	60V	0.3A	5Ω

Chip Size 0.030" × 0.030" (ZVN13/33)

FERRANTI Power MOSFETS will directly interface with MICROPROCESSORS, LOGIC ARRAYS and standard IC LOGIC families including CMOS, TTL, PMOS and NMOS.

PACKAGE DIMENSIONS



PIN OUT	
1	Drain
2	Gate
3	Source

SYMBOL	INCHES		MILLIMETRES	
	MIN	MAX	MIN	MAX
A	.172	.188	4.37	4.77
B	.142	.158	3.61	4.01
C	.475	.525	12.06	13.34
D	.05		1.27	
E	.10		2.54	
F	.016	.019	.406	.495
G	.085	.095	2.16	2.42

Also available with various lead bends and on Tape and Reel.

VN10LP

ABSOLUTE MAXIMUM RATINGS

Parameters	Symbol	Value	Units
Drain-source voltage	V_{DS}	60	V
Continuous drain current (@ $T_A = 25°C$) (@ $T_C = 25°C$)	I_D	0.27 -	A A
Pulse drain current	I_{DM}	3	A
Gate-source voltage	V_{GS}	±20	V
Power dissipation (@ $T_A = 25°C$) (@$T_C = 25°C$)	P_D	0.625 -	W W
Operating/Storage Temperature Range		−55 to +150	°C

ELECTRICAL CHARACTERISTICS (at T = 25°C unless otherwise stated)

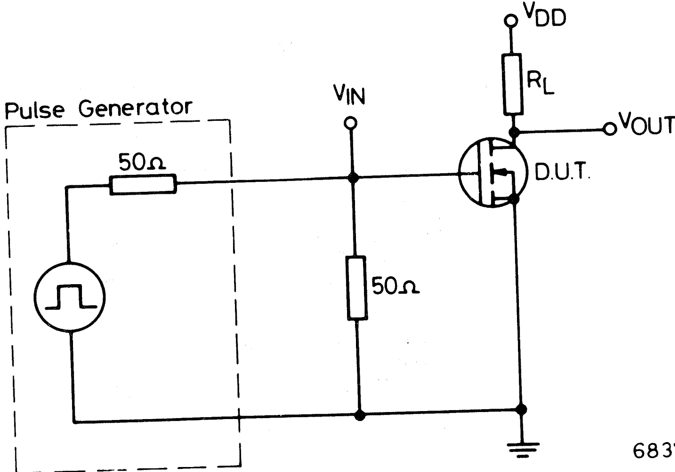
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Drain-source breakdown voltage	BV_{DSS}	60	-	-	V	$I_D = 100\mu A$, $V_{GS} = 0$
Gate-source threshold voltage	$V_{GS(th)}$	0.8	-	2.5	V	$I_D = 1mA$, $V_{DS} = V_{GS}$
Gate-body leakage	I_{GSS}	-	-	100	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0$
Zero gate voltage drain current (Note 2)	I_{DSS}	-	-	10	µA	V_{DS} = max. rating
		-	-	-	mA	$V_{DS} = 0.8 \times$ max. rating $V_{GS} = 0$ (T = 125°)
On-state drain current*	$I_{D(ON)}$	0.75	-	-	A	$V_{DS} = 15V$, $V_{GS} = 10V$
Static drain-source ON-resistance*	$R_{DS(ON)}$	-	-	5	Ω	$I_D = 500mA$, $V_{GS} = 10V$
Forward transconductance* (Note 2)	g_{fs}	100	-	-	mS	$V_{DS} = 15V$, $I_D = 0.5A$
Input capacitance (Note 2)	C_{iss}	-	-	60	pF	$V_D = 25V$ $V_{GS} = 0$ f = 1MHz
Common source output capacitance (Note 2)	C_{oss}	-	-	25	pF	
Reverse transfer capacitance (Note 2)	C_{rss}	-	-	5	pF	
Turn-on time (Notes 1 & 2)	$t_{d(on)}$	-	-	10	n secs	$V_{DD} = 15V$, $I_D \simeq 0.6A$ $R_L = 23\Omega$, $R_g = 25\Omega$
Turn-off time (Notes 1 & 2)	$t_{d(off)}$	-	-	10	n secs	

*Measured under pulsed conditions. Width = 300µS. Duty cycle ≤ 2%.

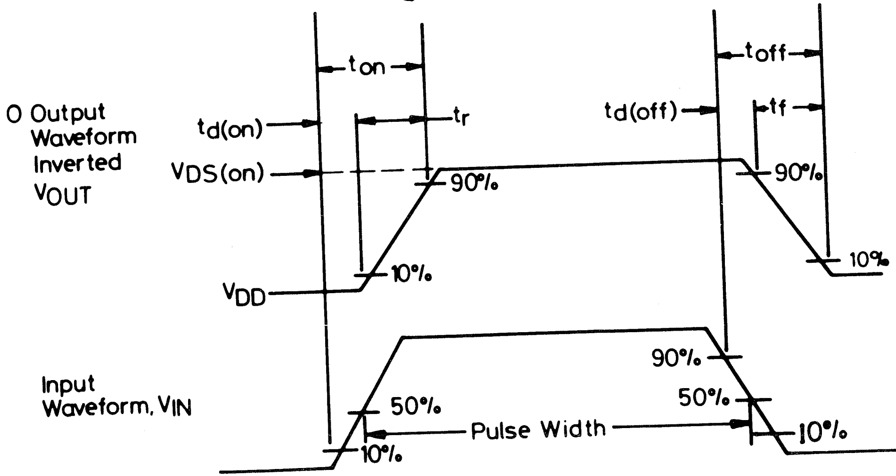
Note 1 Switching times measured with 50ohm source impedance and <5ns rise time on a pulse generator.

Note 2 Sample test.

Circuit for Measuring Switching Times



Switching Waveforms



Note:
Power MOSFET switching
times are essentially independent
of operating temperature

VN10LP

Fig. 1 Saturation Characteristics

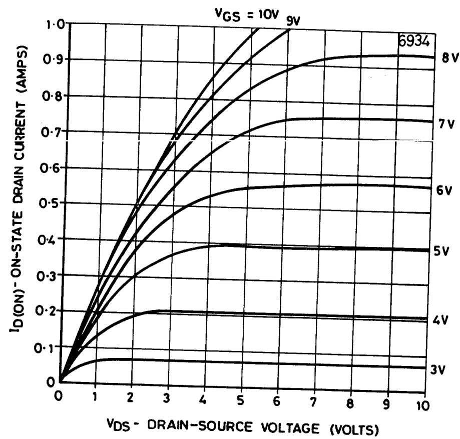


Fig. 2 Voltage Saturation Characteristics

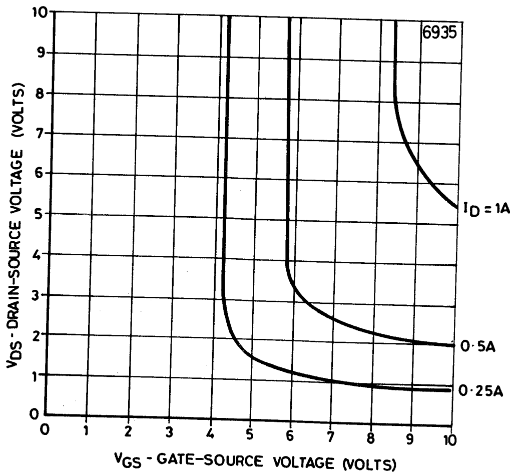


Fig. 3 Transfer Characteristics

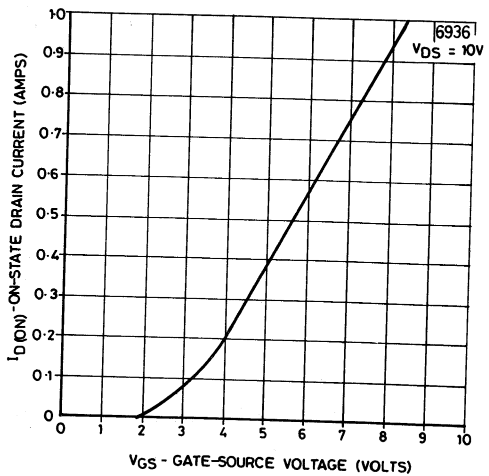


Fig. 4 Capacitance vs Drain-Source Voltage

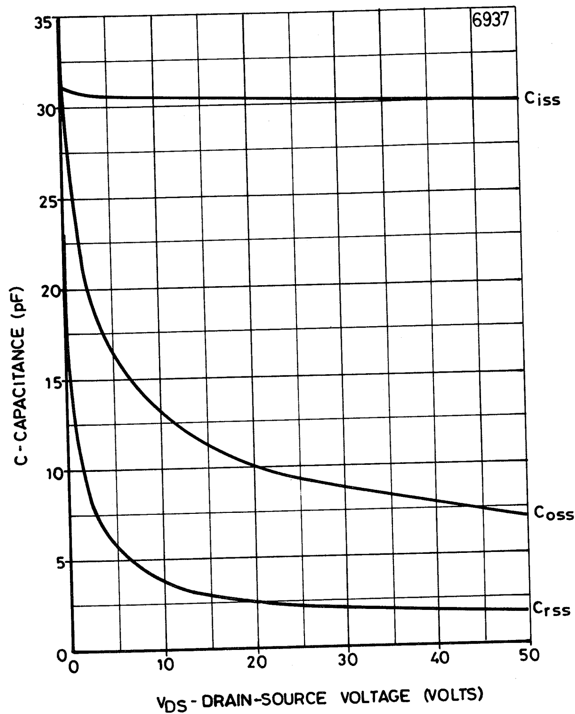


Fig. 5 Transconductance vs Drain-Current

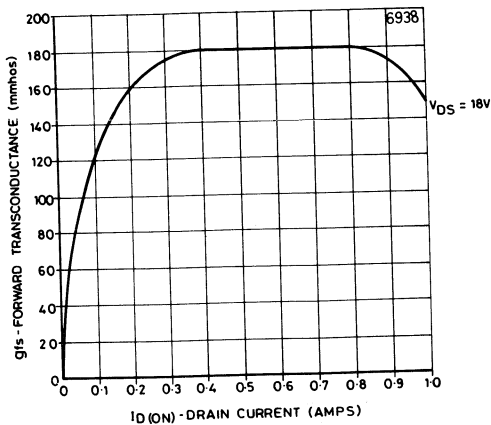
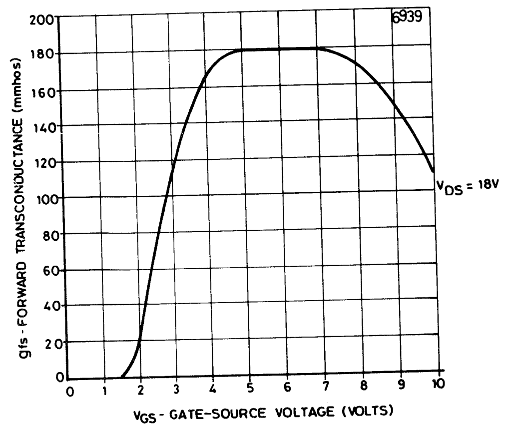


Fig. 6 Transconductance vs Gate-Source Voltage



VN10LP

Fig. 7 Gate Charge vs Gate-Source Voltage

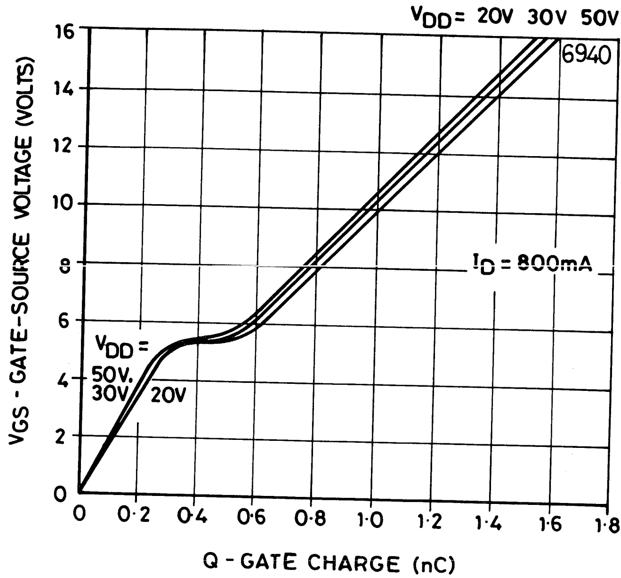


Fig. 8 ON-Resistance vs Gate-Source Voltage

Fig. 9 Variation of $R_{DS(ON)}$ and $V_{GS(th)}$ with Temperature

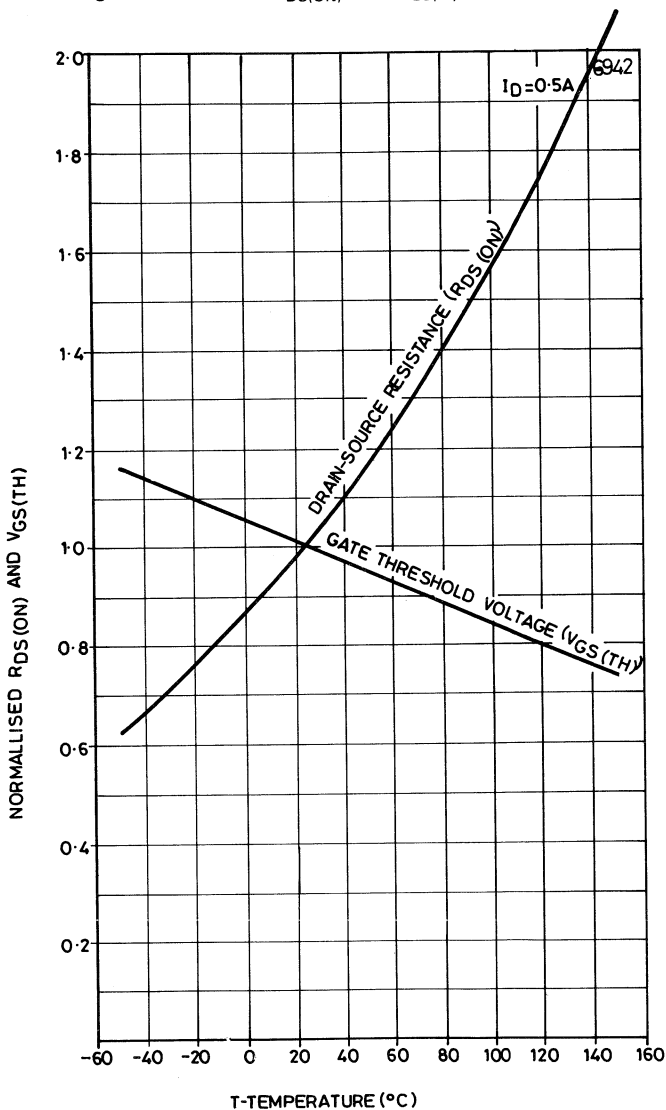
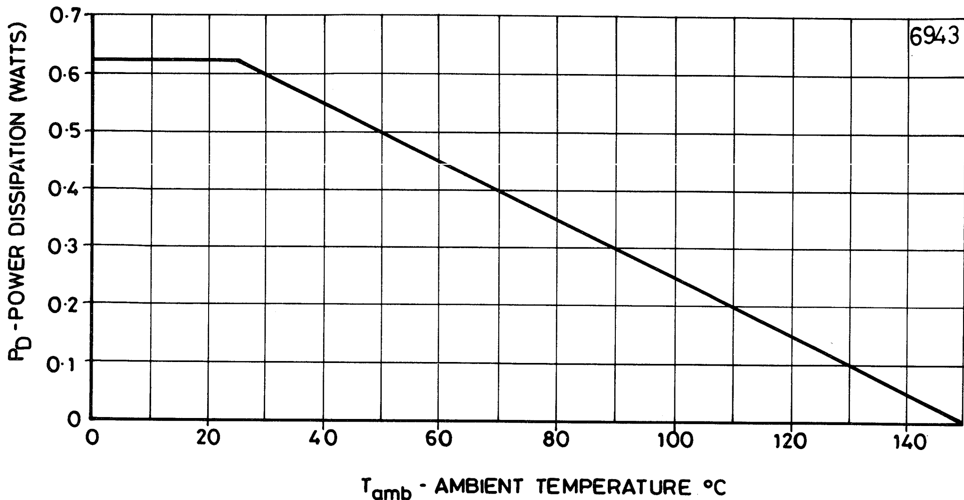


Fig. 10 Power Derating (Ambient)



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Issue 1, May 1984 4.5M

Printed in England CP

Section 2

ZVN21 Range

ZVN2106A/B/L

ZVN2110A/B/L

ZVN0117TA

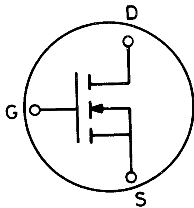
ZVN0120A/B/L

ZVN0102A
ZVN2104A
ZVN2106A

FERRANTI semiconductors®

N-Channel Enhancement-Mode Vertical DMOS Power FET

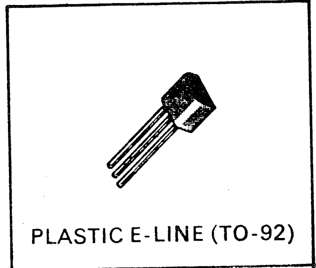
60V: 2 ohm: 0.45A



N-Channel

FEATURES

- Compact Geometry
- Fast Switching Speeds
- No Secondary Breakdown
- Excellent Temperature Stability
- High Input Impedance
- Low Current Drive



PLASTIC E-LINE (TO-92)

DESCRIPTION

Compact OVERLAY (CELL) and INTER-DIGITATED geometries are the basis of the new generation of FERRANTI Power MOSFET transistors. These efficient geometries, optimised for low ON-resistance, low capacitances and fast switching speeds, with computer controlled processing combine to achieve greater device ruggedness.

The planar construction, coupled with ion implantation and the self-aligned poly-silicon gate manufacturing process, provides the reliability and stability in performance required in todays designs.

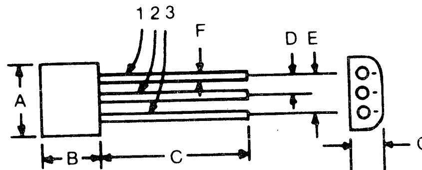
PRODUCT SUMMARY

Device Type	BV_{DSS}	$I_{D(CONT)}$	$R_{D(ON)}$
ZVN0102A	20V	0.45A	2Ω
ZVN2104A	40V	0.45A	2Ω
ZVN2106A	60V	0.45A	2Ω

Chip Size 0.042″ × 0.042″

FERRANTI Power MOSFETS will directly interface with MICROPROCESSORS, LOGIC ARRAYS and standard IC LOGIC families including CMOS, TTL, PMOS and NMOS.

PACKAGE DIMENSIONS



PIN OUT	
1	Drain
2	Gate
3	Source

SYMBOL	INCHES		MILLIMETRES	
	MIN	MAX	MIN	MAX
A	.172	.188	4.37	4.77
B	.142	.158	3.61	4.01
C	.475	.525	12.06	13.34
D	.05		1.27	
E	.10		2.54	
F	.016	.019	.406	.495
G	.085	.095	2.16	2.42

Also available with various lead bends and on Tape and Reel.

ZVN0102A/2104A/2106A

ABSOLUTE MAXIMUM RATINGS

	Parameters	ZVN0102A	ZVN2104A	ZVN2106A	Units
V_{DS}	Drain-source voltage	20	40	60	V
I_D	Continuous drain current (@ $T_A = 25°C$)	0.45			A
I_D	Continuous drain current (@ $T_C = 25°C$)	-			A
I_{DM}	Pulse drain current	8			A
V_{GS}	Gate-source voltage	±20			V
P_D	Max. Power Dissipation (@ $T_A = 25°C$)	0.7			W
P_D	Max. Power Dissipation (@ $T_C = 25°C$)	-			W
	Operating/Storage Temperature Range	−55 to +150			°C

ELECTRICAL CHARACTERISTICS (at T=25°C unless otherwise stated)

Parameter		Symbol	Min.	Typ.	Max.	Unit	Conditions
Drain source breakdown voltage	ZVN0102A	BV_{DSS}	20	-	-	V	$I_D = 1mA$, $V_{GS} = 0$
	ZVN2104A		40	-	-		
	ZVN2106A		60	-	-		
Gate-source threshold voltage		$V_{GS(th)}$	0.8	-	2.4	V	$I_D = 1mA$, $V_{DS} = V_{GS}$
Gate body leakage		I_{GSS}	-	0.1	20	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0$
Zero gate voltage Drain current (Note 2)		I_{DSS}	-	-	0.5	μA	V_{DS} = max. rating, $V_{GS} = 0$
			-	-	0.1	mA	$V_{DS} = 0.8 \times$ max. rating $V_{GS} = 0$ (T=125°C)
On-state drain current*		$I_{D(ON)}$	2	3	-	A	$V_{DS} = 18V$, $V_{GS} = 10V$
Static drain-source ON-resistance*		$R_{DS(ON)}$	-	-	2	Ω	$I_D = 1A$, $V_{GS} = 10V$
Forward transconductance* (Note 2)		g_{fs}	0.3	0.4	-	S	$V_{DS} = 18V$, $I_D = 1A$
Input capacitance (Note 2)		C_{iss}	-	60	75	pF	$V_{DS} = 18V$, $V_{GS} = 0$, f=1MHz
Common source output capacitance (Note 2)		C_{oss}	-	30	45		
Reverse transfer capacitance (Note 2)		C_{rss}	-	15	20		
Turn-ON delay time (Notes 1 & 2)		$t_{d(on)}$	-	4	7	n secs	$V_{DD} = 18V$, $I_D = 1A$
Rise time (Notes 1 & 2)		t_r	-	5	8		
Turn-OFF delay time (Notes 1 & 2)		$t_{d(off)}$	-	8	12		
Fall time (Notes 1 & 2)		t_f	-	10	15		

* Measured under pulsed conditions. Width=300μs. Duty cycle ≤2%.

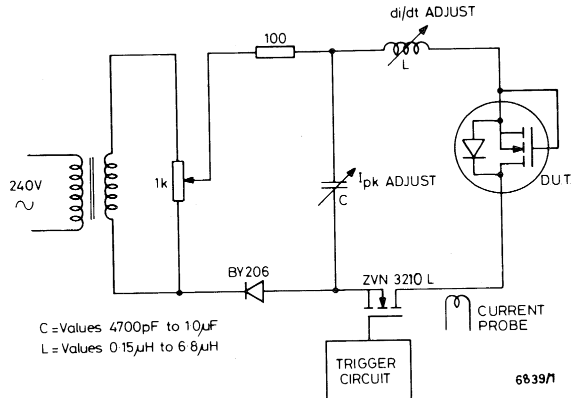
Note 1 Switching times measured with 50 ohm source impedance and <5ns rise time on a pulse generator.

Note 2 Sample test.

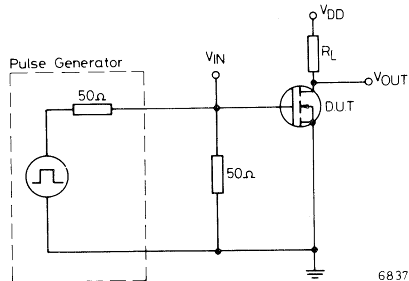
DRAIN-SOURCE DIODE CHARACTERISTICS

Parameter	Symbol	Typ.	Unit	Conditions
Forward ON voltage*	V_{SD}	0.82	V	$V_{GS}=0$, $I_S=0.45A$
Reverse recovery time	t_{rr}	50	n secs	$V_{GS}=0$, $I_F=0.45A$, $I_R=0.1A$

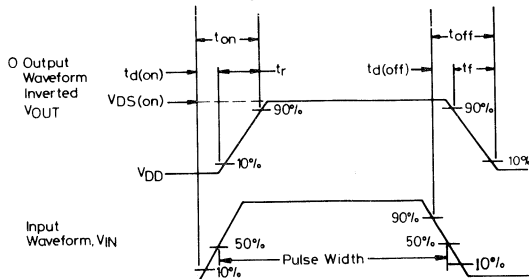
Reverse Recovery Test Circuit



Circuit for Measuring Switching Times



Switching Waveforms



Note:
Power MOSFET switching times are essentially independent of operating temperature

Fig. 1 Saturation Characteristics

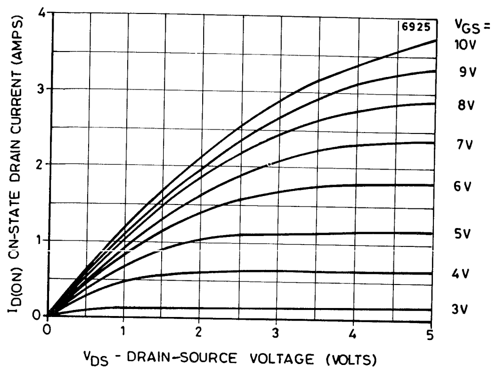


Fig. 2 Voltage Saturation Characteristics

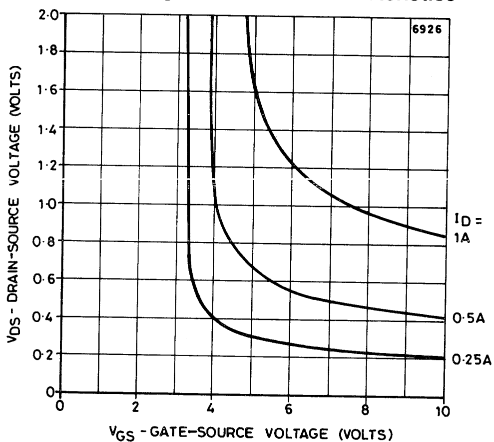


Fig. 3 Transfer Characteristics

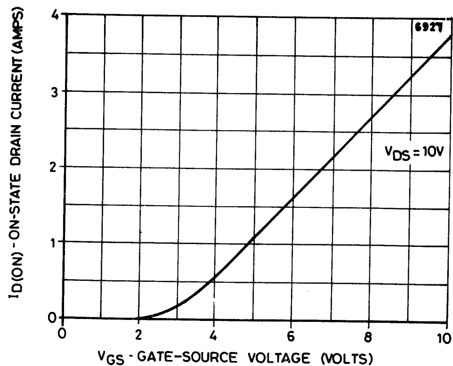


Fig. 4 Capacitance vs Drain-Source Voltage

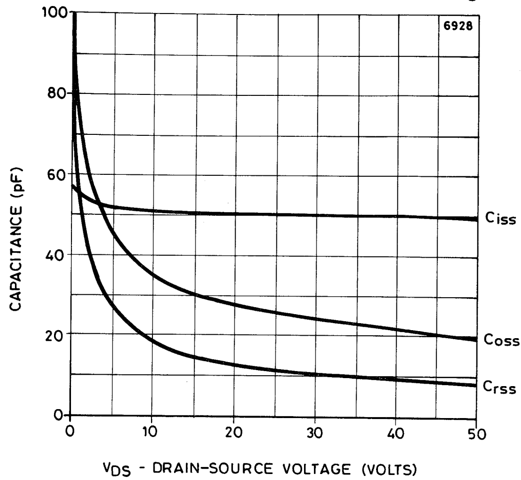


Fig. 5 Transconductance vs Drain-Current

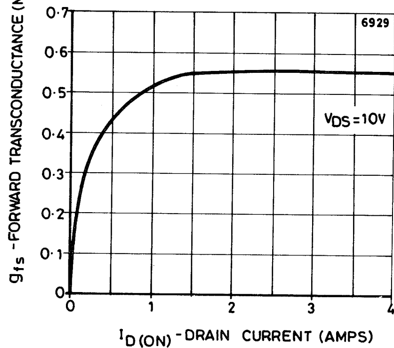
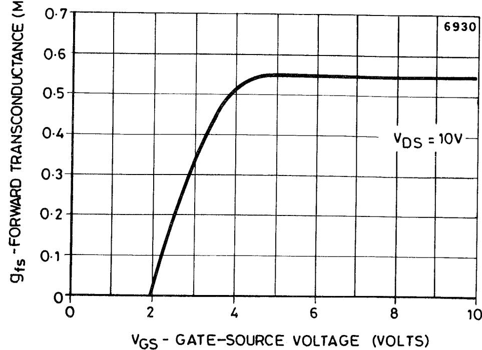


Fig. 6 Transconductance vs Gate-Source Voltage



ZVN0102A/2104A/2106A

Fig. 7 Gate Charge vs Gate-Source Voltage

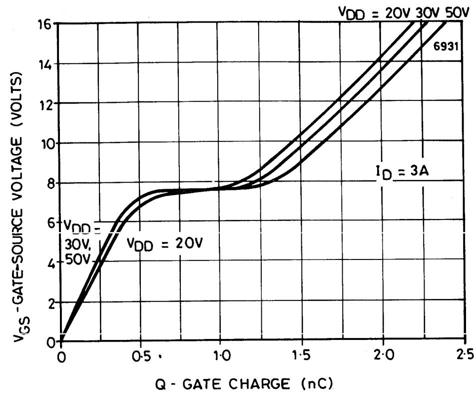


Fig. 8 ON-Resistance vs Gate-Source Voltage

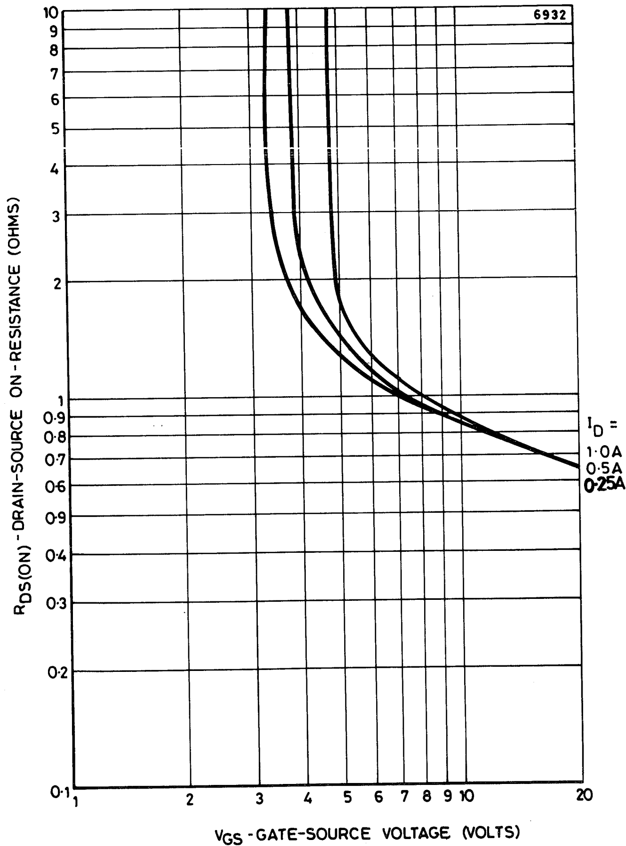


Fig. 9 Variation of $R_{DS(ON)}$ and $V_{GS(th)}$ with Temperature

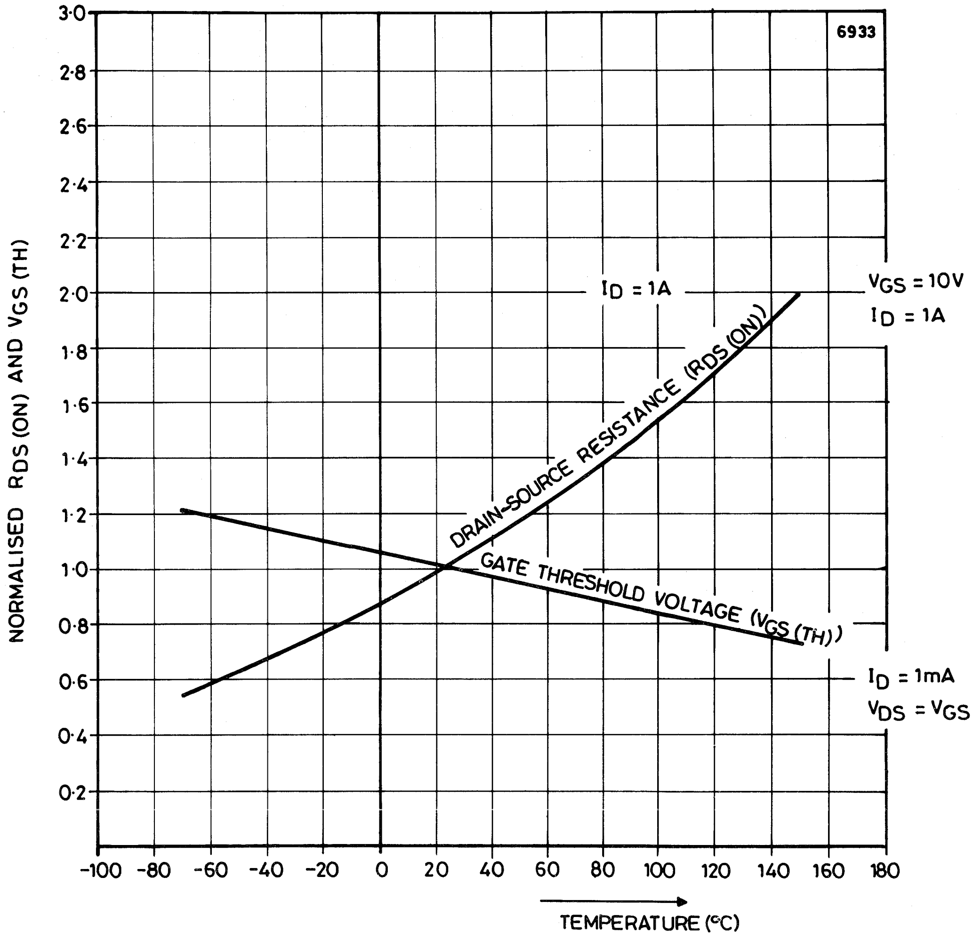
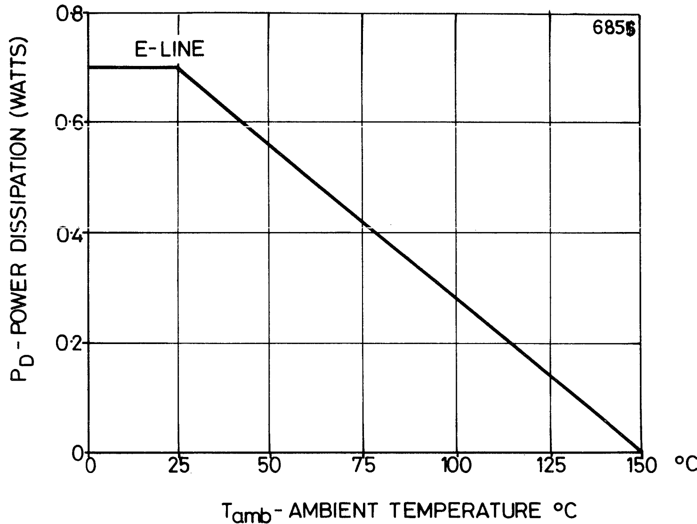


Fig. 10 Power Derating (Ambient)



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Issue 1, May 1984 4.5M

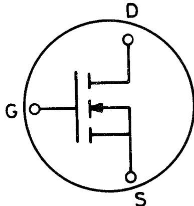
Printed in England CP

FERRANTI semiconductors®

ZVN0102B
ZVN2104B
ZVN2106B

N-Channel Enhancement-Mode Vertical DMOS Power FET

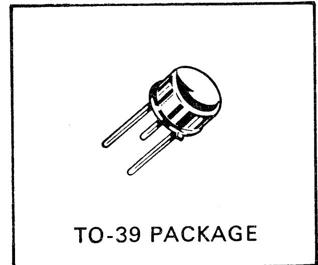
60V: 2 ohm: 1.2A



N-Channel

FEATURES

- Compact Geometry
- Fast Switching Speeds
- No Secondary Breakdown
- Excellent Temperature Stability
- High Input Impedance
- Low Current Drive
- Ease of Paralleling



TO-39 PACKAGE

DESCRIPTION

Compact OVERLAY (CELL) and INTERDIGITATED geometries are the basis of the new generation of FERRANTI Power MOSFET transistors. These efficient geometries, optimised for low ON-resistance, low capacitances and fast switching speeds, with computer controlled processing combine to achieve greater device ruggedness.

The planar construction, coupled with ion implantation and the self-aligned poly-silicon gate manufacturing process, provides the reliability and stability in performance required in todays designs.

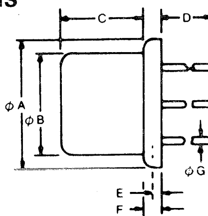
PRODUCT SUMMARY

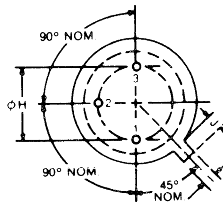
Device Type	BV_{DSS}	$I_{D(CONT)}$	$R_{D(ON)}$
ZVN0102B	20V	1.2A	2Ω
ZVN2104B	40V	1.2A	2Ω
ZVN2106B	60V	1.2A	2Ω

Chip Size 0.042″ × 0.042″

FERRANTI Power MOSFETS will directly interface with MICROPROCESSORS, LOGIC ARRAYS and standard IC LOGIC families including CMOS, TTL, PMOS and NMOS.

PACKAGE DIMENSIONS





PIN OUT	
1	Source
2	Gate
3	Drain & Case

SYMBOL	INCHES		MILLIMETRES	
	MIN	MAX	MIN	MAX
ϕA	.350	.370	8.89	9.40
ϕB	.306	.335	7.77	8.51
C	.240	.260	6.10	6.60
D	.500		12.70	
E	.009	.023	.229	.584
F	.018	.045	.458	1.143
ϕG	.016	.021	.406	.533
ϕH	.190	.210	4.83	5.33
I	.028	.037	.711	.939
J	.026	.040	.660	1.016

ZVN0102B/2104B/2106B

ABSOLUTE MAXIMUM RATINGS

	Parameters	ZVN0102B	ZVN2104B	ZVN2106B	Units
V_{DS}	Drain-source voltage	20	40	60	V
I_D	Continuous drain current (@ $T_A=25°C$)	0.45			A
I_D	Continuous drain current (@ $T_C=25°C$)	1.2			A
I_{DM}	Pulse drain current	8			A
V_{GS}	Gate-source voltage	±20			V
P_D	Max. power dissipation (@ $T_A=25°C$)	0.7			W
P_D	Max. power dissipation (@ $T_C=25°C$)	5			W
	Operating/Storage Temperature Range	−55 to +150			°C

ELECTRICAL CHARACTERISTICS (at T=25°C unless otherwise stated)

Parameter		Symbol	Min.	Typ.	Max.	Unit	Conditions
Drain source breakdown voltage	ZVN0102B	BV_{DSS}	20	-	-	V	$I_D=1mA$, $V_{GS}=0$
	ZVN2104B		40	-	-		
	ZVN2106B		60	-	-		
Gate-source threshold voltage		$V_{GS(th)}$	0.8	-	2.4	V	$I_D=1mA$, $V_{DS}=V_{GS}$
Gate body leakage		I_{GSS}	-	0.1	20	nA	$V_{GS}=\pm20V$, $V_{DS}=0$
Zero gate voltage Drain current (Note 2)		I_{DSS}	-	-	0.5	μA	V_{DS}=max. rating, $V_{GS}=0$
			-	-	0.1	mA	$V_{DS}=0.8 \times$ max. rating $V_{GS}=0$ (T=125°C)
On-state drain current*		$I_{D(ON)}$	2	3	-	A	$V_{DS}=18V$, $V_{GS}=10V$
Static drain-source ON-resistance*		$R_{DS(ON)}$	-	-	2	Ω	$I_D=1A$, $V_{GS}=10V$
Forward transconductance* (Note 2)		g_{fs}	0.3	0.4	-	S	$V_{DS}=18V$, $I_D=1A$
Input capacitance (Note 2)		C_{iss}	-	60	75	pF	$V_{DS}=18V$ $V_{GS}=0$ f=1MHz
Common source output capacitance (Note 2)		C_{oss}	-	30	45	pF	
Reverse transfer capacitance (Note 2)		C_{rss}	-	15	20	pF	
Turn-ON delay time (Notes 1 & 2)		$t_{d(on)}$	-	4	7	n secs	$V_{DD}=18V$ $I_D=1A$
Rise time (Notes 1 & 2)		t_r	-	5	8	n secs	
Turn-OFF delay time (Notes 1 & 2)		$t_{d(off)}$	-	8	12	n secs	
Fall time (Notes 1 & 2)		t_f	-	10	15	n secs	

*Measured under pulsed conditions. Width=300μs. Duty cycle ≤2%.

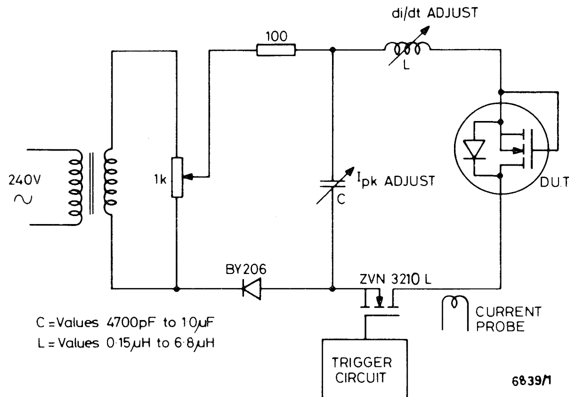
Note 1 Switching times measured with 50 ohm source impedance and <5ns rise time on a pulse generator.

Note 2 Sample test.

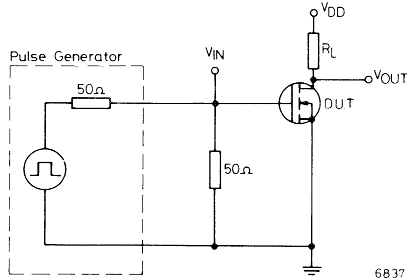
DRAIN-SOURCE DIODE CHARACTERISTICS

Parameter	Symbol	Typ.	Unit	Conditions
Forward ON voltage*	V_{SD}	1.06	V	$V_{GS}=0$, $I_S=1.2A$
Reverse recovery time	t_{rr}	50	n secs	$V_{GS}=0$, $I_F=1.2A$, $I_R=0.1A$

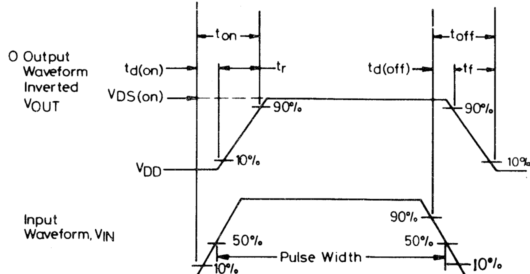
Reverse Recovery Test Circuit



Circuit for Measuring Switching Times



Switching Waveforms



Note:
Power MOSFET switching times are essentially independent of operating temperature

Input voltage amplitude 10 Volts peak

6838/1

Fig. 1 Saturation Characteristics

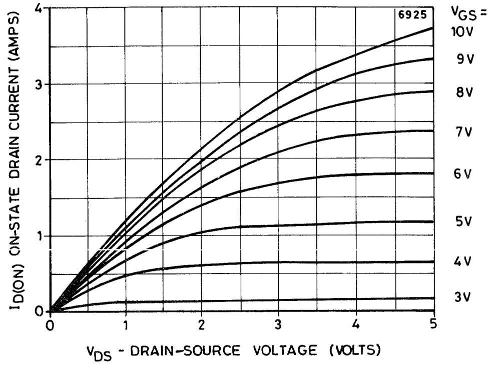


Fig. 2 Voltage Saturation Characteristics

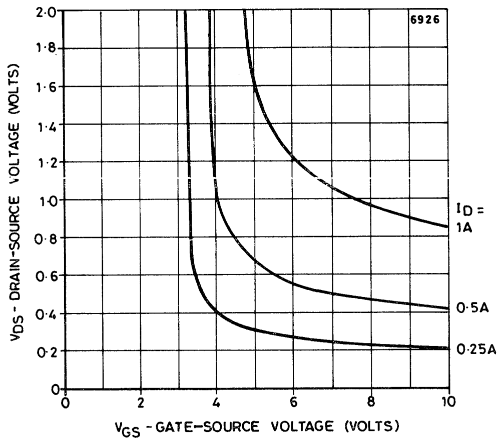


Fig. 3 Transfer Characteristics

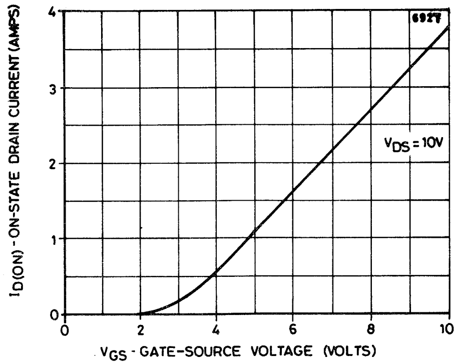


Fig. 4 Capacitance vs Drain-Source Voltage

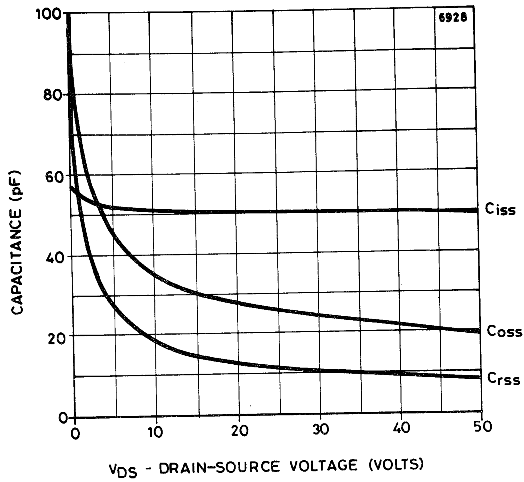


Fig. 5 Transconductance vs Drain-Current

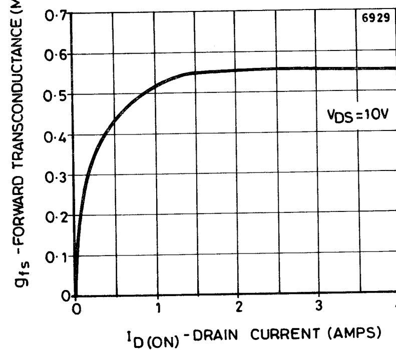


Fig. 6 Transconductance vs Gate-Source Voltage

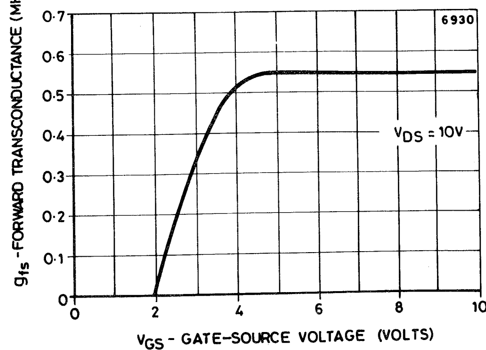


Fig. 7 Gate Charge vs Gate-Source Voltage

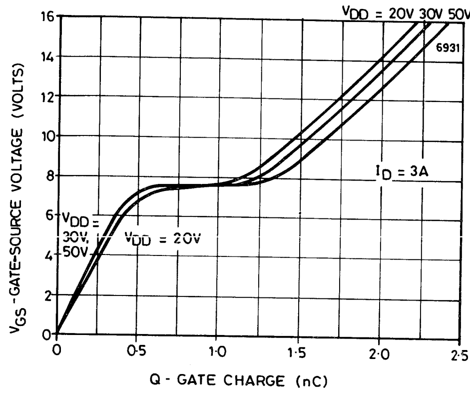


Fig. 8 ON-Resistance vs Gate-Source Voltage

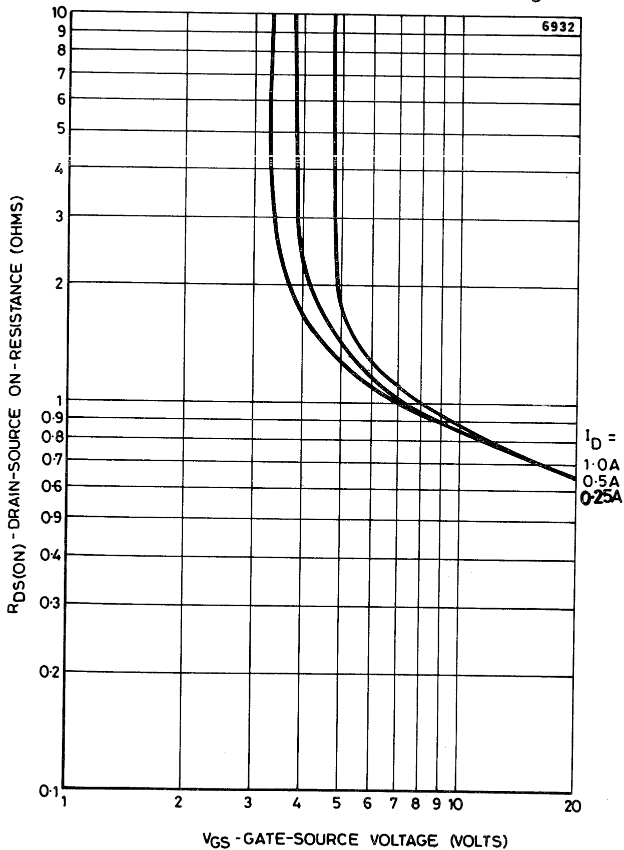
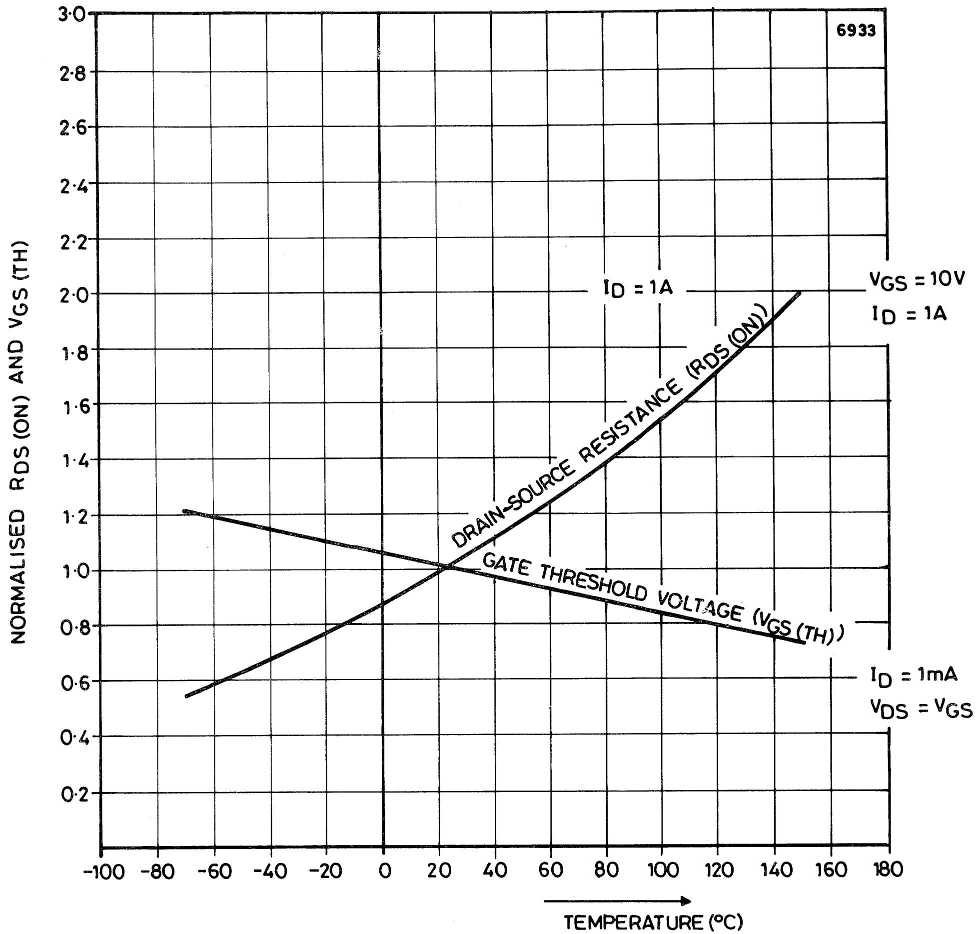


Fig. 9 Variation of $R_{DS(ON)}$ and $V_{GS(th)}$ with Temperature



ZVN0102B/2104B/2106B

Fig. 10 Power Derating (Case)

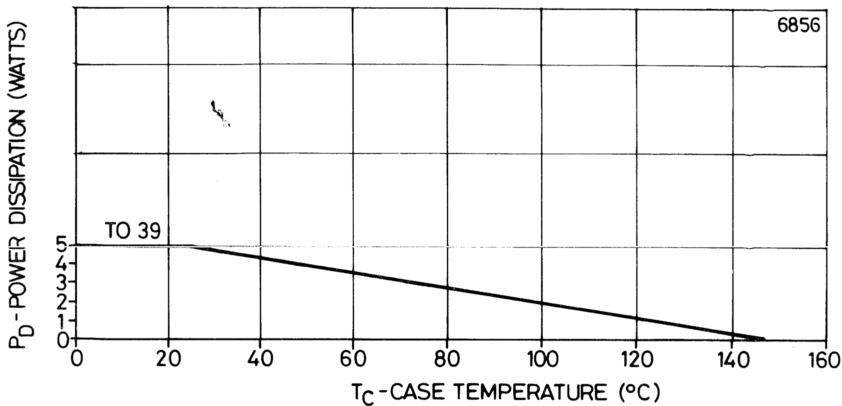
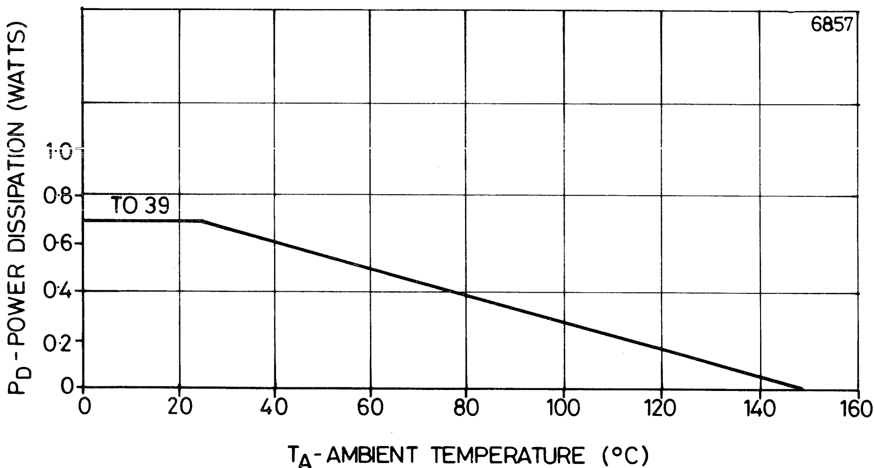


Fig. 11 Power Derating (Ambient)



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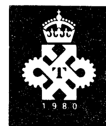

Issue 1, May 1984 4.5M

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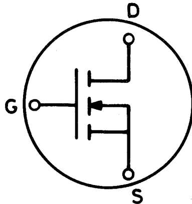
FERRANTI semiconductors ®

ZVN0102L
ZVN2104L
ZVN2106L

N-Channel Enhancement-Mode Vertical DMOS Power FET

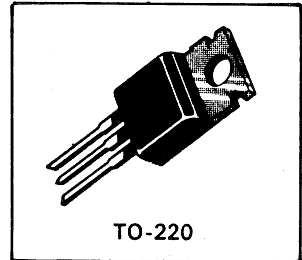
60V: 2 ohm: 2A



N-Channel

FEATURES

- Compact Geometry
- Fast Switching Speeds
- No Secondary Breakdown
- Excellent Temperature Stability
- High Input Impedance
- Low Current Drive
- Ease of Paralleling



TO-220

DESCRIPTION

Compact OVERLAY (CELL) and INTER-DIGITATED geometries are the basis of the new generation of FERRANTI Power MOSFET transistors. These efficient geometries, optimised for low ON-resistance, low capacitances and fast switching speeds, with computer controlled processing combine to achieve greater device ruggedness.

The planar construction, coupled with ion implantation and the self-aligned poly-silicon gate manufacturing process, provides the reliability and stability in performance required in todays designs.

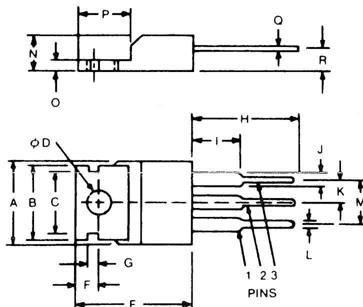
PRODUCT SUMMARY

Device Type	BV_{DSS}	$I_{D(CONT)}$	$R_{D(ON)}$
ZVN0102L	20V	2A	2Ω
ZVN2104L	40V	2A	2Ω
ZVN2106L	60V	2A	2Ω

Chip Size 0.042" × 0.042"

FERRANTI Power MOSFETS will directly interface with MICROPROCESSORS, LOGIC ARRAYS and standard IC LOGIC families including CMOS, TTL, PMOS and NMOS.

PACKAGE DIMENSIONS



PIN OUT	
1	Gate
2	Drain & Tab
3	Source

SYMBOL	INCHES		MILLIMETRES	
	MIN	MAX	MIN	MAX
A	.380	.420	9.65	10.66
B	.380	.420	9.65	10.66
C	.300	.320	7.62	8.12
ϕD	.139	.147	3.531	3.733
E	.560	.625	14.230	15.870
F	.100	.120	2.54	3.04
G	.040	.060	1.02	1.52
H	.500	.562	12.70	14.27
I		.250		6.35
J	.045	.060	1.14	1.52
K	.090	.110	2.29	2.79
L	.020	.040	.510	1.016
M	.190	.210	4.830	5.330
N	.175	.185	4.445	4.699
O	.030	.055	.762	1.390
P	.230	.270	5.850	6.850
Q	.015	.025	.380	.630
R	.080	.115	2.040	2.920

ZVN0102L/2104L/2106L

ABSOLUTE MAXIMUM RATINGS

	Parameters	ZVN0102L	ZVN2104L	ZVN2106L	Units
V_{DS}	Drain-source voltage	20	40	60	V
I_D	Continuous drain current (@ $T_A=25°C$)	0.65			A
I_D	Continuous drain current (@ $T_C=25°C$)	2			A
I_{DM}	Pulse drain current	8			A
V_{GS}	Gate-source voltage	±20			V
P_D	Max. power dissipation (@ $T_A=25°C$)	1.5			W
P_D	Max. power dissipation (@ $T_C=25°C$)	20			W
	Operating/Storage Temperature Range	−55 to +150			°C

ELECTRICAL CHARACTERISTICS (at T=25°C unless otherwise stated)

Parameter		Symbol	Min.	Typ.	Max.	Unit	Conditions
Drain source breakdown voltage	ZVN0102L	BV_{DSS}	20	-	-	V	$I_D=1mA$, $V_{GS}=0$
	ZVN2104L		40	-	-		
	ZVN2106L		60	-	-		
Gate-source threshold voltage		$V_{GS(th)}$	0.8	-	2.4	V	$I_D=1mA$, $V_{DS}=V_{GS}$
Gate body leakage		I_{GSS}	-	0.1	20	nA	$V_{GS}=\pm 20V$, $V_{DS}=0$
Zero gate voltage Drain current (Note 2)		I_{DSS}	-	-	0.5	μA	V_{DS}=max. rating, $V_{GS}=0$
			-	-	0.1	mA	$V_{DS}=0.8\times$ max. rating $V_{GS}=0$ (T=125°C)
On-state drain current*		$I_{D(ON)}$	2	3	-	A	$V_{DS}=18V$, $V_{GS}=10V$
Static drain-source ON-resistance*		$R_{DS(ON)}$	-	-	2	Ω	$I_D=1A$, $V_{GS}=10V$
Forward transconductance* (Note 2)		g_{fs}	0.3	0.4	-	S	$V_{DS}=18V$, $I_D=1A$
Input capacitance (Note 2)		C_{iss}	-	60	75	pF	$V_{DS}=18V$ $V_{GS}=0$ f=1MHz
Common source output capacitance (Note 2)		C_{oss}	-	30	45		
Reverse transfer capacitance (Note 2)		C_{rss}	-	15	20		
Turn-ON delay time (Notes 1 & 2)		$t_{d(on)}$	-	4	7	n secs	$V_{DD}=18V$ $I_D=1A$
Rise time (Notes 1 & 2)		t_r	-	5	8		
Turn-OFF delay time (Notes 1 & 2)		$t_{d(off)}$	-	8	12		
Fall time (Notes 1 & 2)		t_f	-	10	15		

*Measured under pulsed conditions. Width=300μs. Duty cycle ⩽2%.

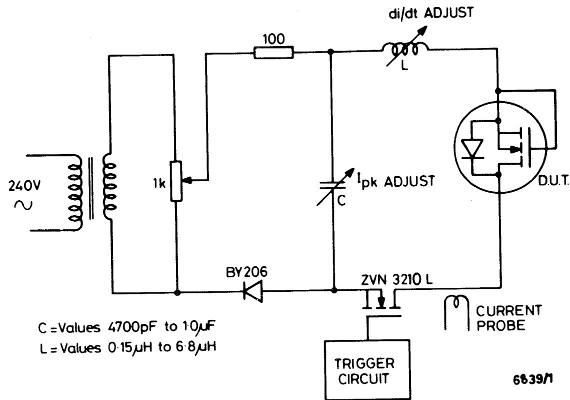
Note 1 Switching times measured with 50 ohm source impedance and <5ns rise time on a pulse generator.

Note 2 Sample test.

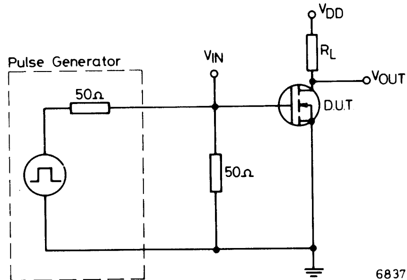
DRAIN-SOURCE DIODE CHARACTERISTICS

Parameter	Symbol	Typ.	Unit	Conditions
Forward ON voltage*	V_{SD}	1	V	$V_{GS}=0$, $I_S=2A$
Reverse recovery time	t_{rr}	38	n secs	$V_{GS}=0$, $I_F=2A$, $I_R=0.1A$

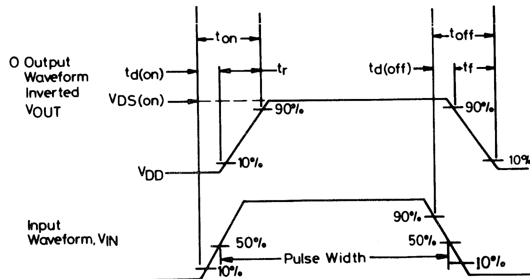
Reverse Recovery Test Circuit



Circuit for Measuring Switching Times



Switching Waveforms



Note:
Power MOSFET switching times are essentially independent of operating temperature

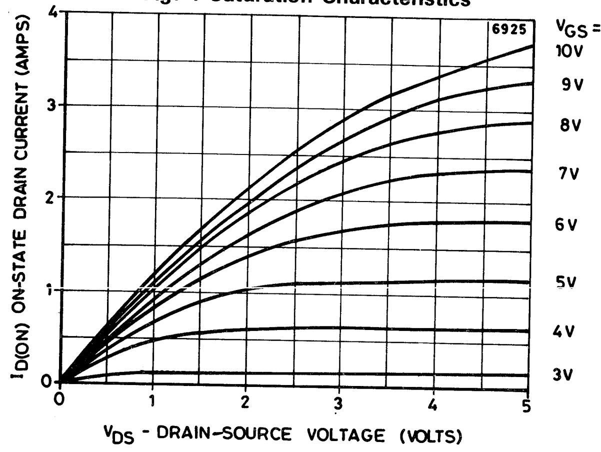


Fig. 1 Saturation Characteristics
6925
V_{GS} =
10V
9V
8V
7V
6V
5V
4V
3V
$I_{D(ON)}$ ON-STATE DRAIN CURRENT (AMPS)
0
1
2
3
4
5
V_{DS} - DRAIN-SOURCE VOLTAGE (VOLTS)

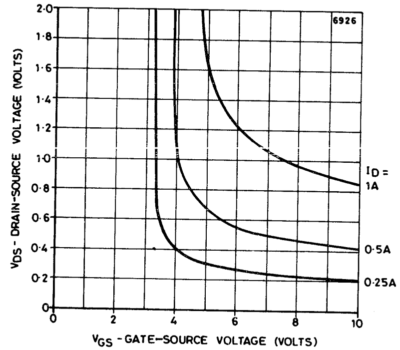


Fig. 2 Voltage Saturation Characteristics
6926
V_{DS} - DRAIN-SOURCE VOLTAGE (VOLTS)
2·0
1·8
1·6
1·4
1·2
1·0
0·8
0·6
0·4
0·2
0
I_D =
1A
0·5A
0·25A
2
4
6
8
10
V_{GS} - GATE-SOURCE VOLTAGE (VOLTS)

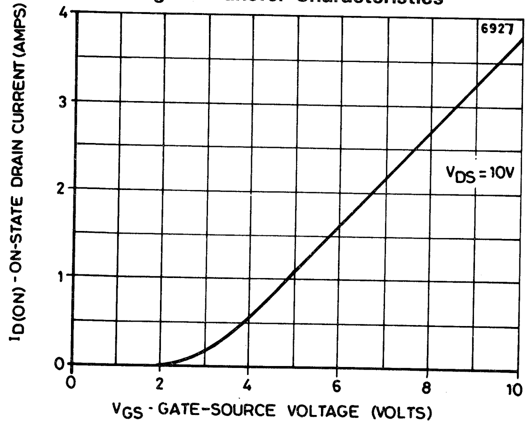


Fig. 3 Transfer Characteristics
6927
V_{DS} = 10V
$I_{D(ON)}$ - ON-STATE DRAIN CURRENT (AMPS)
0
1
2
3
4
6
8
10
V_{GS} - GATE-SOURCE VOLTAGE (VOLTS)

Fig. 4 Capacitance vs Drain-Source Voltage

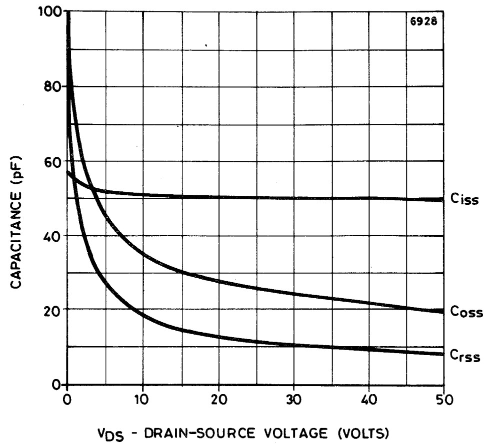


Fig. 5 Transconductance vs Drain-Current

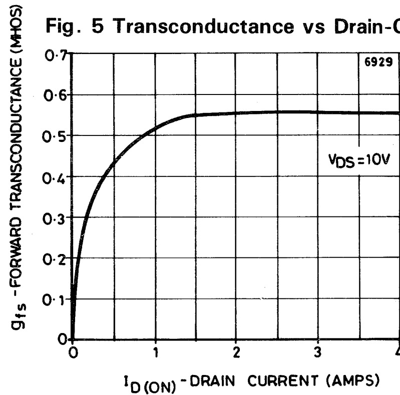


Fig. 6 Transconductance vs Gate-Source Voltage

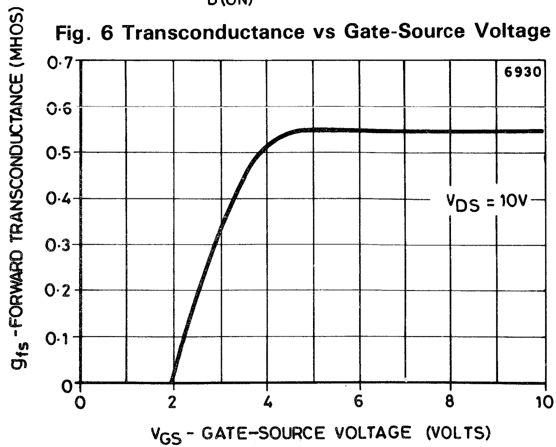


Fig. 7 Gate Charge vs Gate-Source Voltage

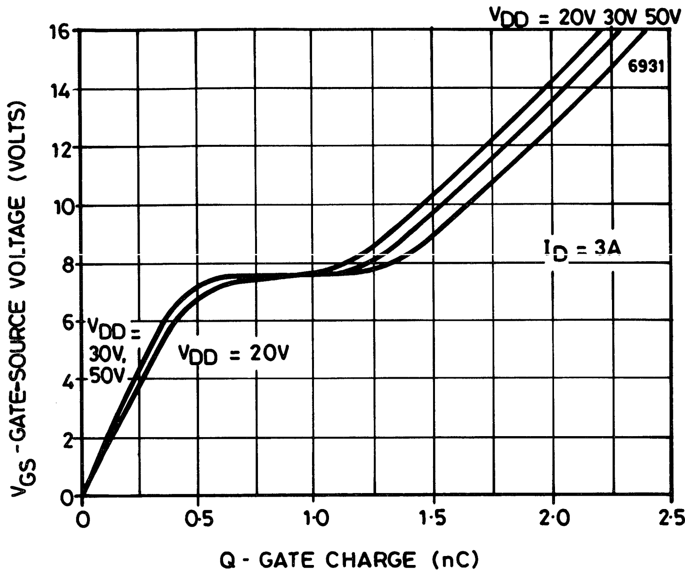


Fig. 8 ON-Resistance vs Gate-Source Voltage

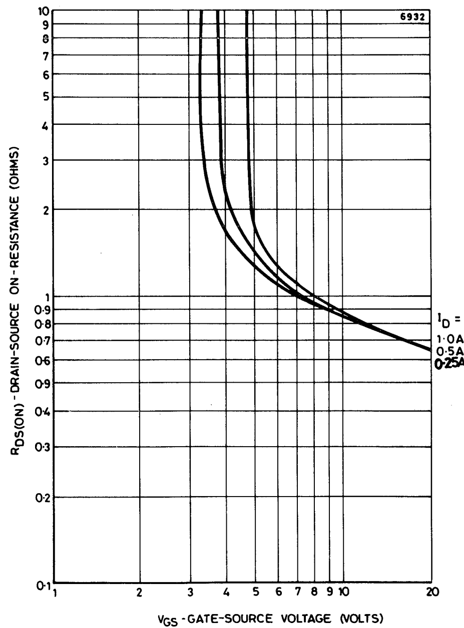


Fig. 9 Variation of $R_{DS(ON)}$ and $V_{GS(th)}$ with Temperature

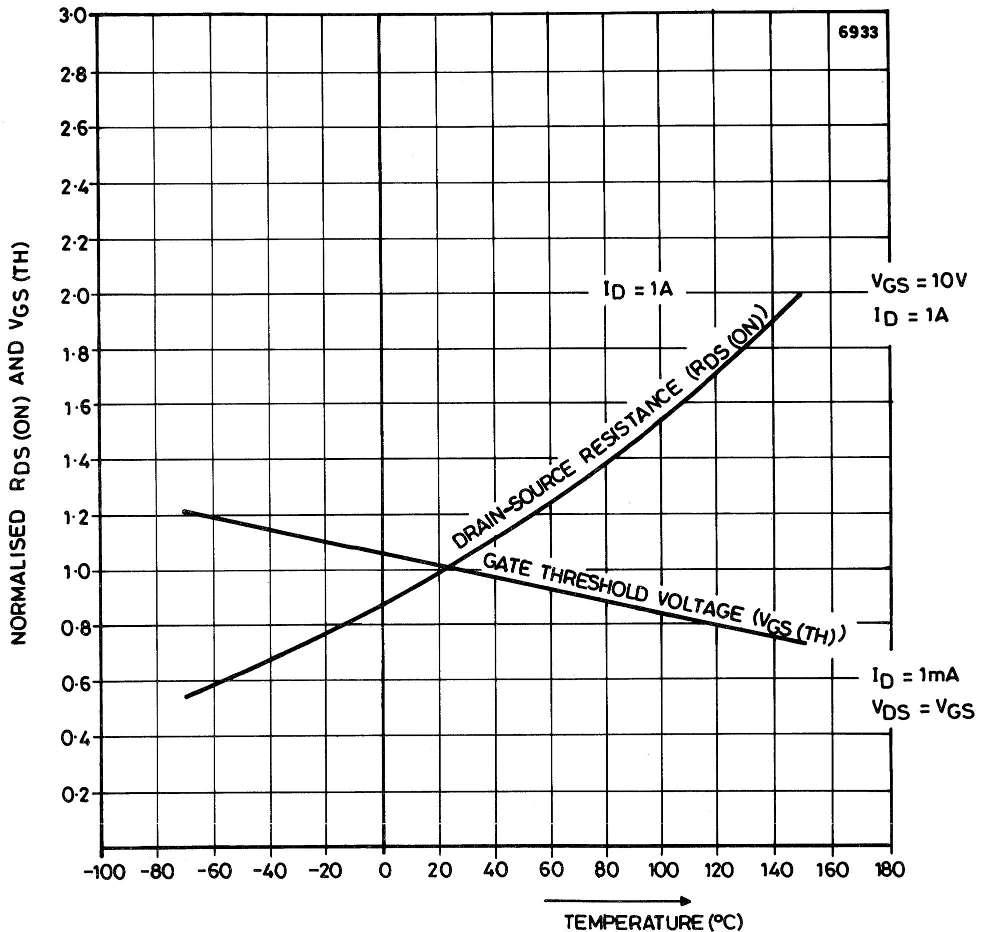


Fig. 10 Power Derating (Case)

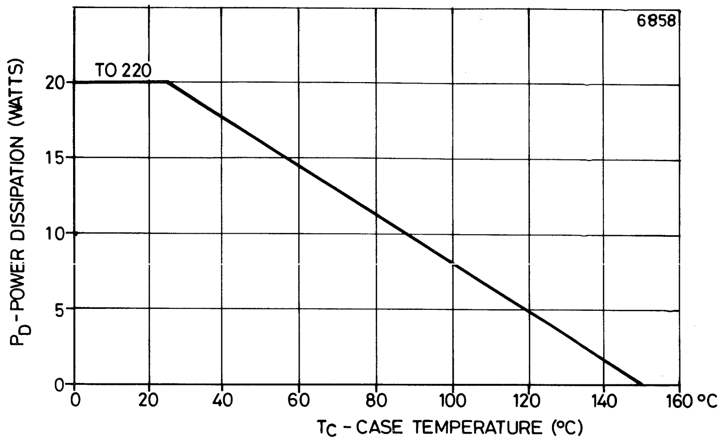
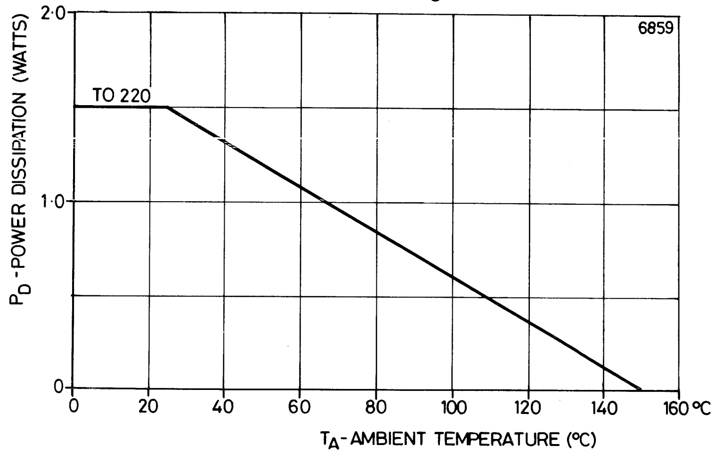


Fig. 11 Power Derating (Ambient)



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Issue 1, May 1984 4.5M

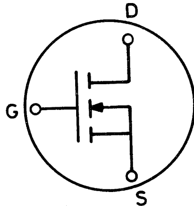
Printed in England CP

ZVN0106A
ZVN0108A
ZVN2110A

FERRANTI semiconductors ®

N-Channel Enhancement-Mode Vertical DMOS Power FET

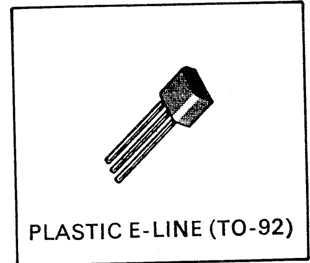
100V: 4 ohm: 0.32A



N-Channel

FEATURES

- Compact Geometry
- Fast Switching Speeds
- No Secondary Breakdown
- Excellent Temperature Stability
- High Input Impedance
- Low Current Drive
- Ease of Paralleling



PLASTIC E-LINE (TO-92)

DESCRIPTION

Compact OVERLAY (CELL) and INTER-DIGITATED geometries are the basis of the new generation of FERRANTI Power MOSFET transistors. These efficient geometries, optimised for low ON-resistance, low capacitances and fast switching speeds, with computer controlled processing combine to achieve greater device ruggedness.

The planar construction, coupled with ion implantation and the self-aligned poly-silicon gate manufacturing process, provides the reliability and stability in performance required in todays designs.

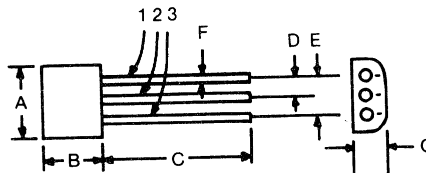
PRODUCT SUMMARY

Device Type	BV_{DSS}	$I_{D(CONT)}$	$R_{D(ON)}$
ZVN0106A	60V	0.32A	4Ω
ZVN0108A	80V	0.32A	4Ω
ZVN2110A	100V	0.32A	4Ω

Chip Size 0.042″ × 0.042″

FERRANTI Power MOSFETS will directly interface with MICROPROCESSORS, LOGIC ARRAYS and standard IC LOGIC families including CMOS, TTL, PMOS and NMOS.

PACKAGE DIMENSIONS



PIN OUT	
1	Drain
2	Gate
3	Source

Also available with various lead bends and on Tape and Reel.

SYMBOL	INCHES		MILLIMETRES	
	MIN	MAX	MIN	MAX
A	.172	.188	4.37	4.77
B	.142	.158	3.61	4.01
C	.475	.525	12.06	13.34
D	.05		1.27	
E	.10		2.54	
F	.016	.019	.406	.495
G	.085	.095	2.16	2.42

ZVN0106A/0108A/2110A

ABSOLUTE MAXIMUM RATINGS

	Parameters	ZVN0106A	ZVN0108A	ZVN2110A	Units
V_{DS}	Drain-source voltage	60	80	100	V
I_D	Continuous drain current (@ $T_A = 25°C$)	0.32			A
I_D	Continuous drain current (@ $T_C = 25°C$)				A
I_{DM}	Pulse drain current	6			A
V_{GS}	Gate-source voltage	±20			V
P_D	Max. power dissipation (@ $T_A = 25°C$)	0.7			W
P_D	Max. power dissipation (@ $T_C = 25°C$)	-			W
	Operating/Storage Temperature Range	−55 to +150			°C

ELECTRICAL CHARACTERISTICS (at T = 25°C unless otherwise stated)

Parameter		Symbol	Min.	Typ.	Max.	Unit	Conditions
Drain-source breakdown voltage	ZVN0106A	BV_{DSS}	60	-	-	V	$I_D = 1mA$, $V_{GS} = 0$
	ZVN0108A		80	-	-		
	ZVN2110A		100	-	-		
Gate-source threshold voltage		$V_{GS(th)}$	0.8	-	2.4	V	$I_D = 1mA$, $V_{DS} = V_{GS}$
Gate-body leakage		I_{GSS}	-	0.1	20	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0$
Zero gate voltage Drain current	(Note 2)	I_{DSS}	-	-	1	μA	V_{DS} = max. rating, $V_{GS} = 0$
			-	-	100	μA	$V_{DS} = 0.8 \times$ max. rating $V_{GS} = 0$ (T = 125°C)
On-state drain current*		$I_{D(ON)}$	1.5	2	-	A	$V_{DS} = 25V$, $V_{GS} = 10V$
Static drain-source ON-resistance*		$R_{DS(ON)}$	-	-	4	Ω	$I_D = 1A$, $V_{GS} = 10V$
Forward transconductance*	(Note 2)	g_{fs}	0.25	0.35	-	S	$V_{DS} = 25V$, $I_D = 1A$
Input capacitance	(Note 2)	C_{iss}	-	59	75	pF	$V_{DS} = 25V$, $V_{GS} = 0$, f = 1MHz
Common source output capacitance	(Note 2)	C_{oss}	-	16	25	pF	
Reverse transfer capacitance	(Note 2)	C_{rss}	-	4	8	pF	
Turn-ON delay time	(Notes 1 & 2)	$t_{d(on)}$	-	4	7	n secs	$V_{DD} = 25V$, $I_D = 1A$
Rise time	(Notes 1 & 2)	t_r	-	4	8	n secs	
Turn-OFF delay time	(Notes 1 & 2)	$t_{d(off)}$	-	8	13	n secs	
Fall time	(Notes 1 & 2)	t_f	-	8	13	n secs	

*Measured under pulsed conditions. Width = 300μs. Duty cycle ⩽ 2%.

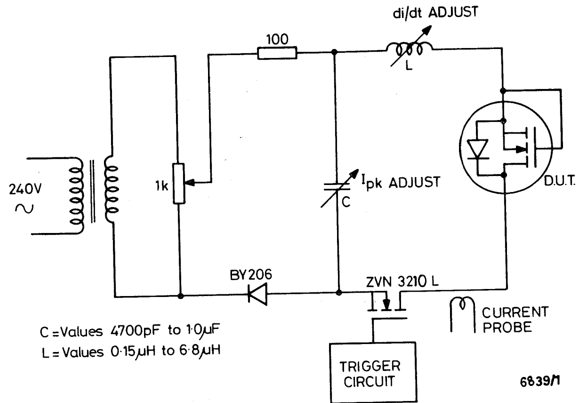
Note 1 Switching times measured with 50 ohm source impedance and <5ns rise time on a pulse generator.

Note 2 Sample test.

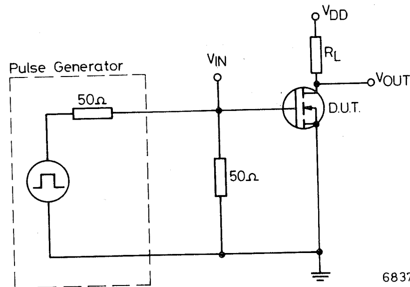
DRAIN-SOURCE DIODE CHARACTERISTICS

Parameter	Symbol	Typ.	Unit	Conditions
Forward ON voltage*	V_{SD}	0.82	V	$V_{GS}=0$, $I_S=320mA$
Reverse recovery time	t_{rr}	112	n secs	$V_{GS}=0$, $I_F=320mA$, $I_R=100mA$

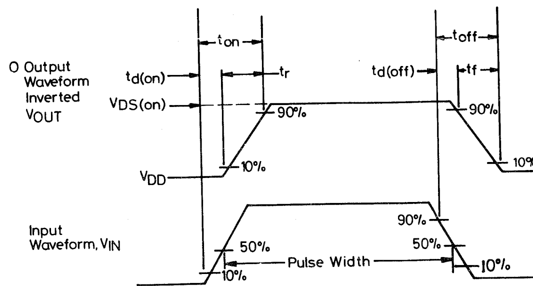
Reverse Recovery Test Circuit



Circuit for Measuring Switching Times



Switching Waveforms



Note:
Power MOSFET switching times are essentially independent of operating temperature

6838/1

Fig. 1 Output Characteristics

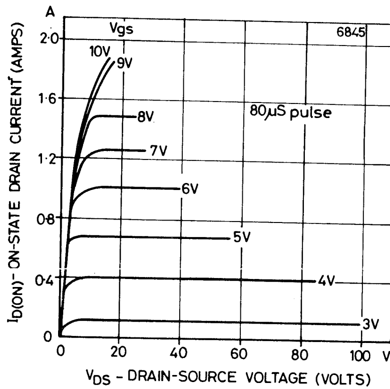


Fig. 2 Saturation Characteristics

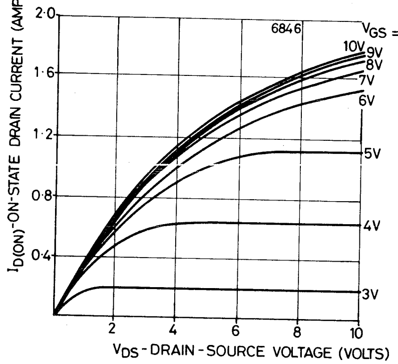


Fig. 3 Voltage Saturation Characteristics

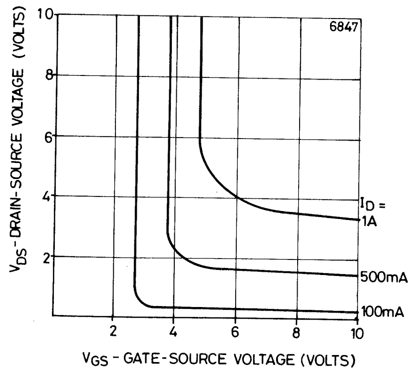


Fig. 4 Transfer Characteristics

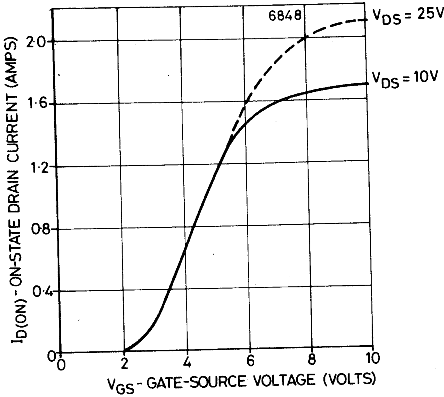


Fig. 5 Capacitance vs Drain-Source Voltage

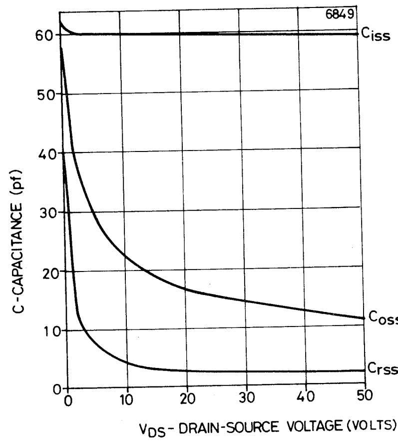


Fig. 6 Transconductance vs Drain Current

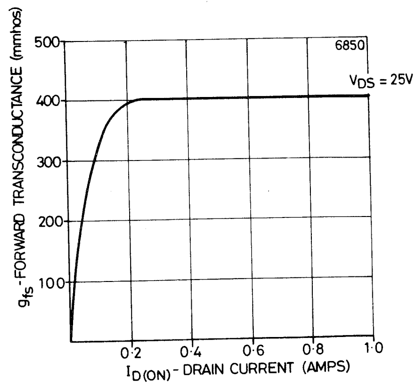


Fig. 7 Transconductance vs Gate-Source Voltage

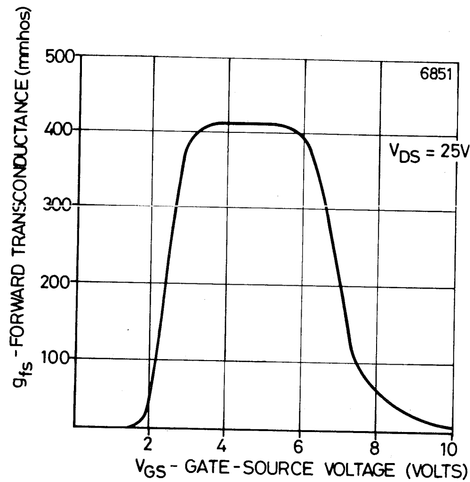


Fig. 8 Gate Charge vs Gate-Source Voltage

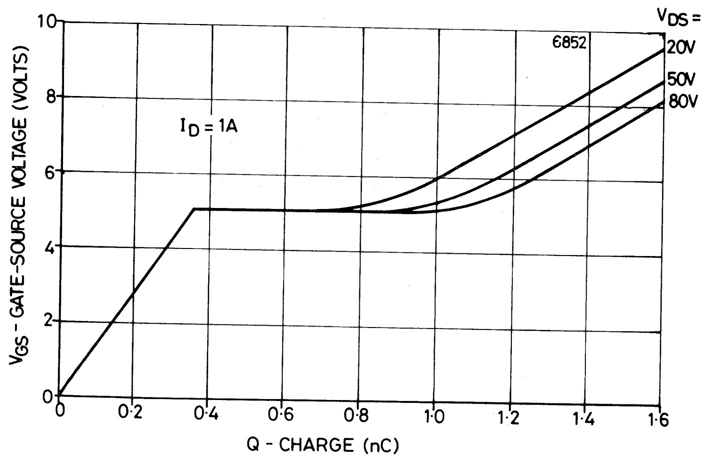


Fig. 9 ON-Resistance vs Gate-Source Voltage

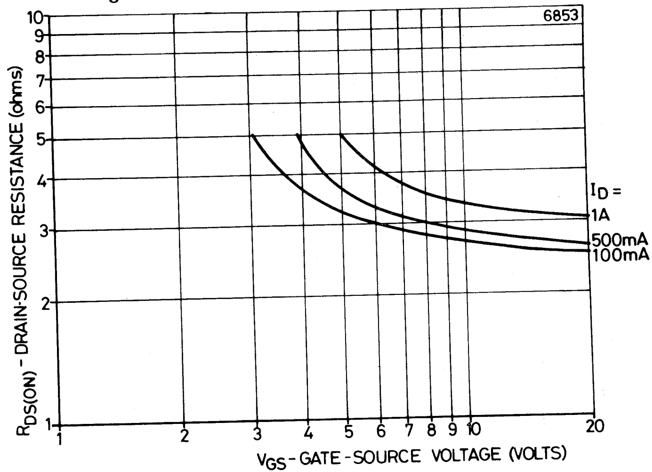
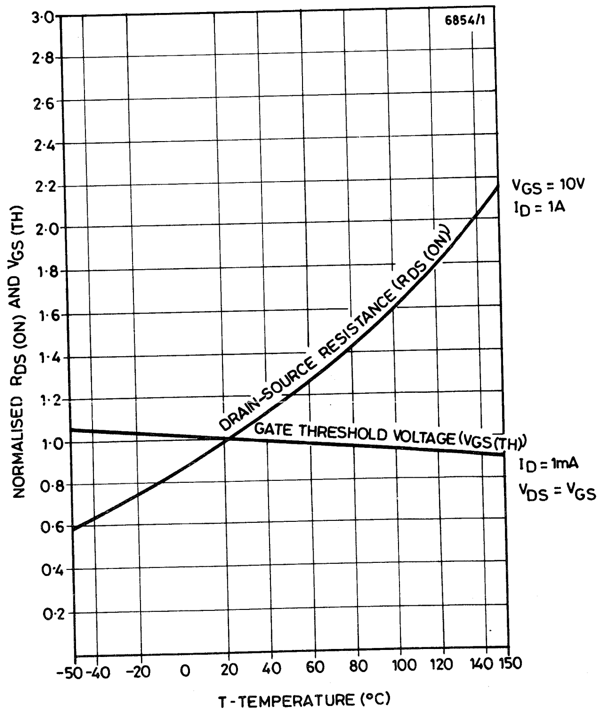
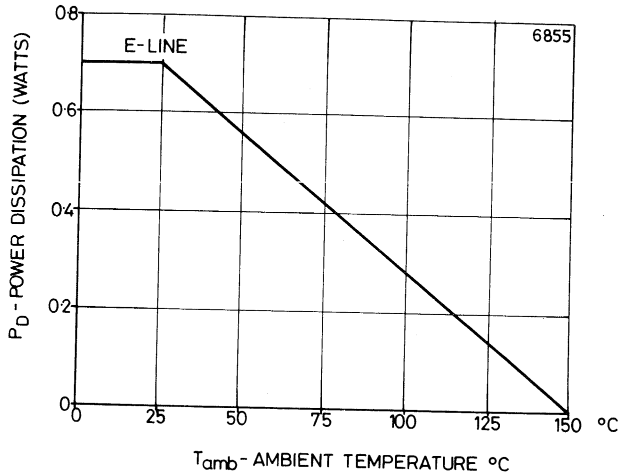


Fig. 10 Variation of $R_{DS(ON)}$ and $V_{GS(th)}$ with Temperature



ZVN0106A/0108A/2110A

Fig. 11 Power Derating (Ambient)



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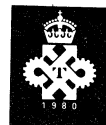
Gee Chang Hong Centre, Aberdeen, Hong Kong Tel: 5-538298-9 Telex: HX 74605



Issue 2, April 1984 4.5M

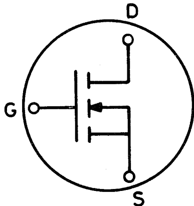
Printed in England CP

ZVN0106B
ZVN0108B
ZVN2110B

FERRANTI semiconductors ®

N-Channel Enhancement-Mode Vertical DMOS Power FET

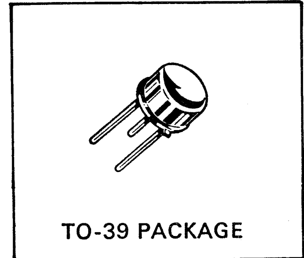
100V: 4 ohm: 0.85A



N-Channel

FEATURES

- Compact Geometry
- Fast Switching Speeds
- No Secondary Breakdown
- Excellent Temperature Stability
- High Input Impedance
- Low Current Drive
- Ease of Paralleling



TO-39 PACKAGE

DESCRIPTION

Compact OVERLAY (CELL) and INTER-DIGITATED geometries are the basis of the new generation of FERRANTI Power MOSFET transistors. These efficient geometries, optimised for low ON-resistance, low capacitances and fast switching speeds, with computer controlled processing combine to achieve greater device ruggedness.

The planar construction, coupled with ion implantation and the self-aligned poly-silicon gate manufacturing process, provides the reliability and stability in performance required in todays designs.

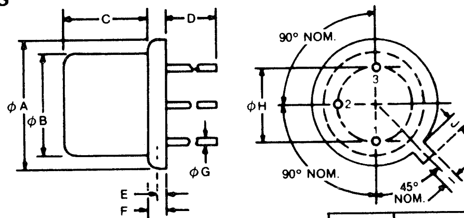
PRODUCT SUMMARY

Device Type	BV_{DSS}	$I_{D(CONT)}$	$R_{D(ON)}$
ZVN0106B	60V	0.85A	4Ω
ZVN0108B	80V	0.85A	4Ω
ZVN2110B	100V	0.85A	4Ω

Chip Size 0.042″ × 0.042″

FERRANTI Power MOSFETS will directly interface with MICROPROCESSORS, LOGIC ARRAYS and standard IC LOGIC families including CMOS, TTL, PMOS and NMOS.

PACKAGE DIMENSIONS



PIN OUT	
1	Source
2	Gate
3	Drain & Case

SYMBOL	INCHES		MILLIMETRES	
	MIN	MAX	MIN	MAX
φA	.350	.370	8.89	9.40
φB	.306	.335	7.77	8.51
C	.240	.260	6.10	6.60
D	.500		12.70	
E	.009	.023	.229	.584
F	.018	.045	.458	1.143
φG	.016	.021	.406	.533
φH	.190	.210	4.83	5.33
I	.028	.037	.711	.939
J	.026	.040	.660	1.016

ZVN0106B/0108B/2110B

ABSOLUTE MAXIMUM RATINGS

	Parameters	ZVN0106B	ZVN0108B	ZVN2110B	Units
V_{DS}	Drain-source voltage	60	80	100	V
I_D	Continuous drain current (@ $T_A = 25°C$)	0.32			A
I_D	Continuous drain current (@ $T_C = 25°C$)	0.85			A
I_{DM}	Pulse drain current	6			A
V_{GS}	Gate-source voltage	±20			V
P_D	Max. power dissipation (@ $T_A = 25°C$)	0.7			W
P_D	Max. power dissipation (@ $T_C = 25°C$)	5			W
	Operating/Storage Temperature Range	−55 to +150			°C

ELECTRICAL CHARACTERISTICS (at T = 25°C unless otherwise stated)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Drain-source breakdown voltage ZVN0106B	BV_{DSS}	60	-	-	V	$I_D = 1mA$, $V_{GS} = 0$
Drain-source breakdown voltage ZVN0108B	BV_{DSS}	80	-	-	V	
Drain-source breakdown voltage ZVN2110B	BV_{DSS}	100	-	-	V	
Gate-source threshold voltage	$V_{GS(th)}$	0.8	-	2.4	V	$I_D = 1mA$, $V_{DS} = V_{GS}$
Gate-body leakage	I_{GSS}	-	0.1	20	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0$
Zero gate voltage Drain current (Note 2)	I_{DSS}	-	-	1	μA	V_{DS} = max. rating, $V_{GS} = 0$
		-	-	100	μA	$V_{DS} = 0.8 \times$ max. rating $V_{GS} = 0$ ($T = 125°C$)
On-state drain current*	$I_{D(ON)}$	1.5	2	-	A	$V_{DS} = 25V$, $V_{GS} = 10V$
Static drain-source ON-resistance*	$R_{DS(ON)}$	-	-	4	Ω	$I_D = 1A$, $V_{GS} = 10V$
Forward transconductance* (Note 2)	g_{fs}	0.25	0.35	-	S	$V_{DS} = 25V$, $I_D = 1A$
Input capacitance (Note 2)	C_{iss}	-	59	75	pF	$V_{DS} = 25V$
Common source output capacitance (Note 2)	C_{oss}	-	16	25	pF	$V_{GS} = 0$
Reverse transfer capacitance (Note 2)	C_{rss}	-	4	8	pF	$f = 1MHz$
Turn-ON delay time (Notes 1 & 2)	$t_{d(on)}$	-	4	7	n secs	$V_{DD} = 25V$
Rise time (Notes 1 & 2)	t_r	-	4	8	n secs	
Turn-OFF delay time (Notes 1 & 2)	$t_{d(off)}$	-	8	13	n secs	$I_D = 1A$
Fall time (Notes 1 & 2)	t_f	-	8	13	n secs	

*Measured under pulsed conditions. Width = 300μs. Duty cycle ≤ 2%.

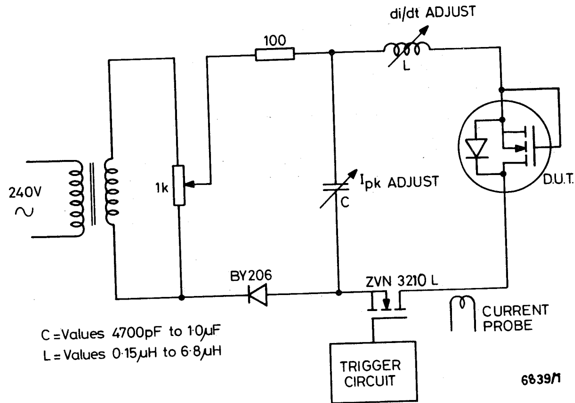
Note 1 Switching times measured with 50 ohm source impedance and <5ns rise time on a pulse generator.

Note 2 Sample test.

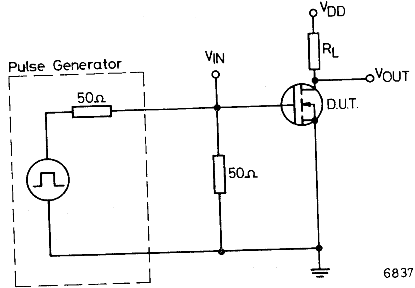
DRAIN-SOURCE DIODE CHARACTERISTICS

Parameter	Symbol	Typ.	Unit	Conditions
Forward ON voltage*	V_{SD}	0.85	V	$V_{GS}=0$, $I_S=850mA$
Reverse recovery time	t_{rr}	126	n secs	$V_{GS}=0$, $I_F=850mA$, $I_R=100mA$

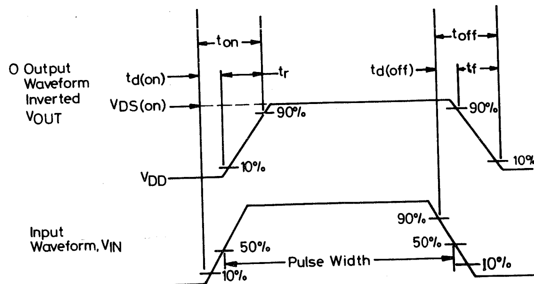
Reverse Recovery Test Circuit



Circuit for Measuring Switching Times



Switching Waveforms



Note:
Power MOSFET switching times are essentially independent of operating temperature

ZVN0106B/0108B/2110B

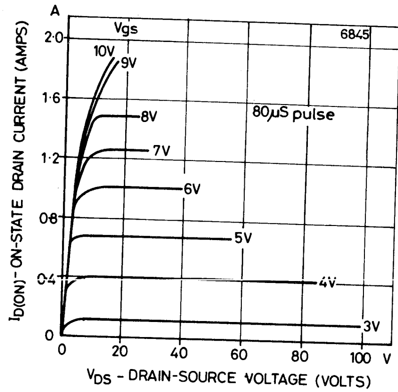


Fig. 1 Output Characteristics

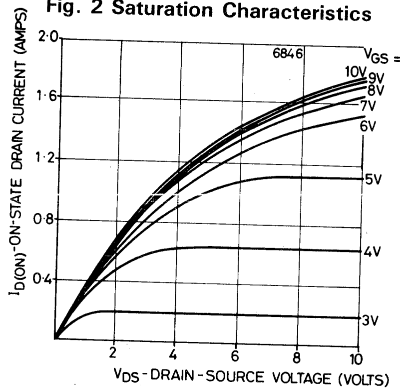


Fig. 2 Saturation Characteristics

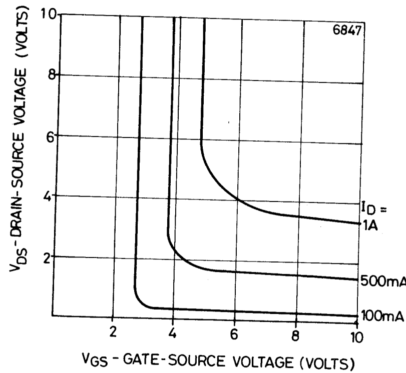


Fig. 3 Voltage Saturation Characteristics

Fig. 4 Transfer Characteristics

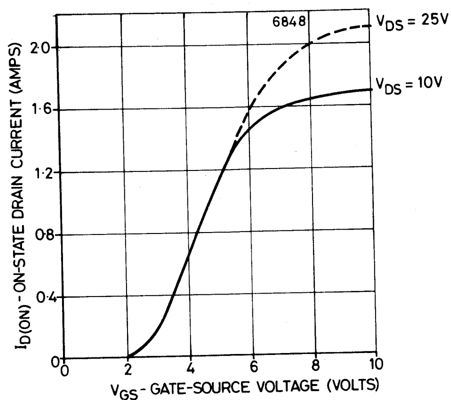


Fig. 5 Capacitance vs Drain-Source Voltage

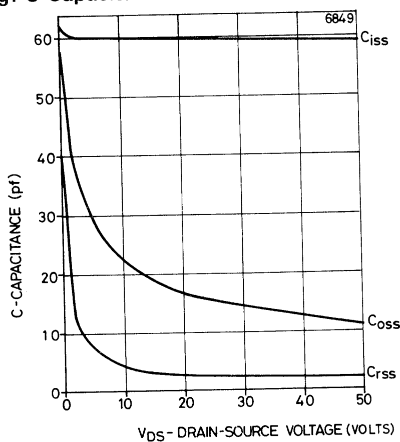


Fig. 6 Transconductance vs Drain Current.

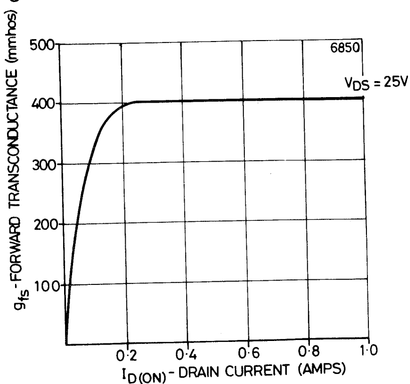


Fig. 7 Transconductance vs Gate-Source Voltage

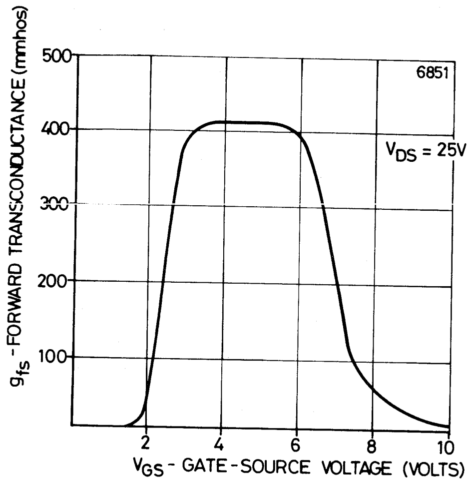


Fig. 8 Gate Charge vs Gate-Source Voltage

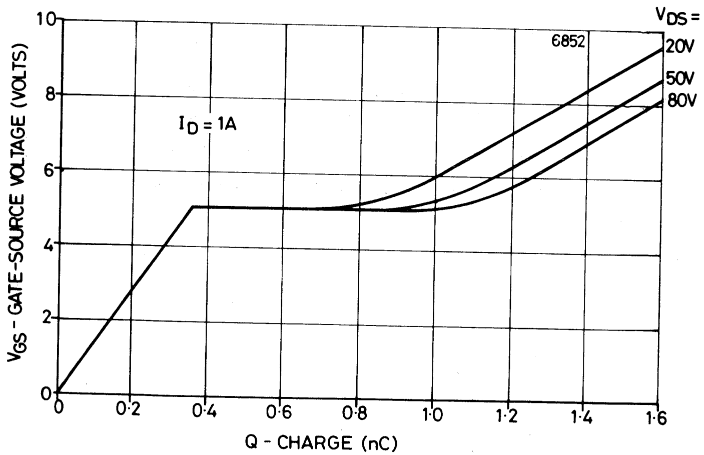


Fig. 9 ON-Resistance vs Gate-Source Voltage

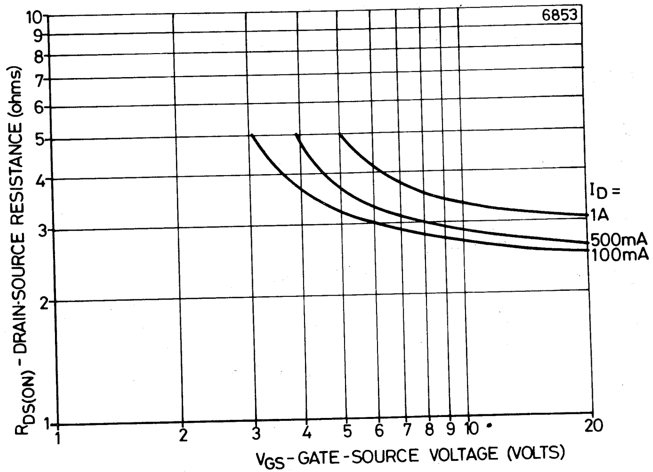


Fig. 10 Variation of $R_{DS(ON)}$ and $V_{GS(th)}$ with Temperature

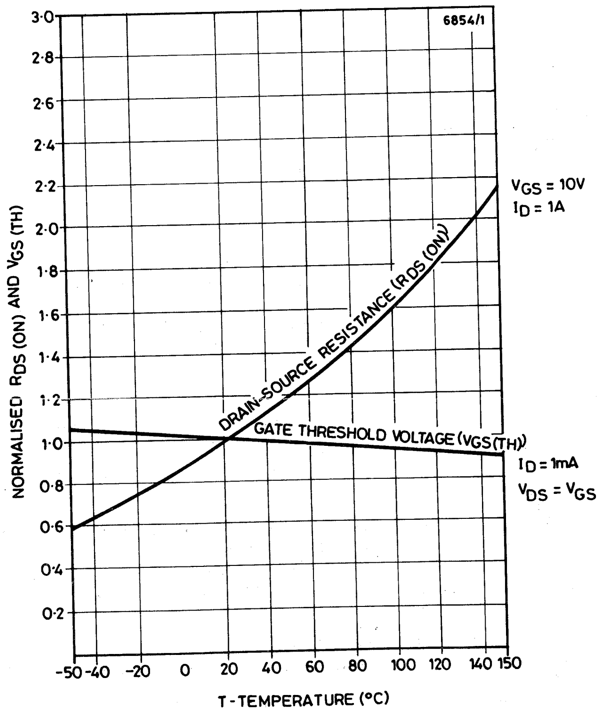


Fig. 11 Power Derating (Case)

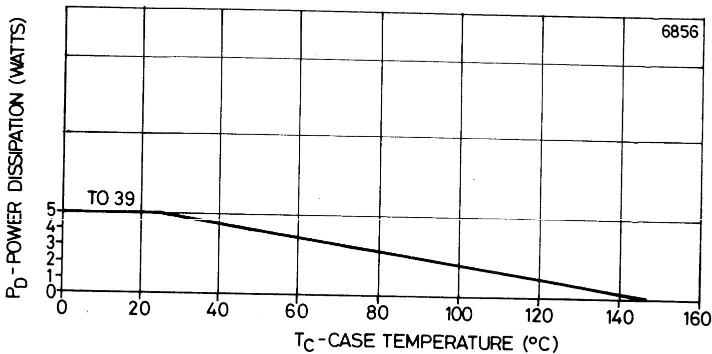
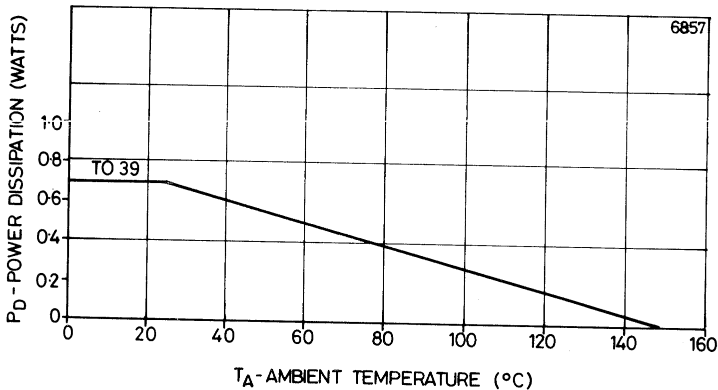


Fig. 12 Power Derating (Ambient)



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Issue 2, April 1984 4.5M

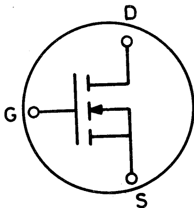
Printed in England CP

ZVN0106L
ZVN0108L
ZVN2110L

FERRANTI semiconductors ®

N-Channel Enhancement-Mode Vertical DMOS Power FET

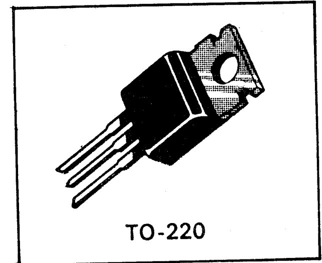
100V: 4 ohm: 1.5A



N-Channel

FEATURES

- Compact Geometry
- Fast Switching Speeds
- No Secondary Breakdown
- Excellent Temperature Stability
- High Input Impedance
- Low Current Drive
- Ease of Paralleling



TO-220

DESCRIPTION

Compact OVERLAY (CELL) and INTER-DIGITATED geometries are the basis of the new generation of FERRANTI Power MOSFET transistors. These efficient geometries, optimised for low ON-resistance, low capacitances and fast switching speeds, with computer controlled processing combine to achieve greater device ruggedness.

The planar construction, coupled with ion implantation and the self-aligned poly-silicon gate manufacturing process, provides the reliability and stability in performance required in todays designs.

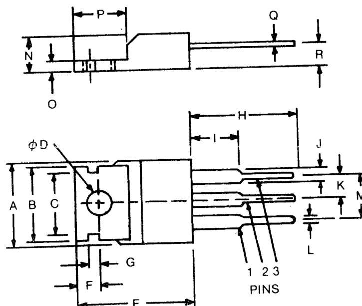
PRODUCT SUMMARY

Device Type	BV_{DSS}	$I_{D(CONT)}$	$R_{D(ON)}$
ZVN0106L	60V	1.5A	4Ω
ZVN0108L	80V	1.5A	4Ω
ZVN2110L	100V	1.5A	4Ω

Chip Size 0.042″ × 0.042″

FERRANTI Power MOSFETS will directly interface with MICROPROCESSORS, LOGIC ARRAYS and standard IC LOGIC families including CMOS, TTL, PMOS and NMOS.

PACKAGE DIMENSIONS



PIN OUT	
1	Gate
2	Drain & Tab
3	Source

SYMBOL	INCHES		MILLIMETRES	
	MIN	MAX	MIN	MAX
A	.380	.420	9.65	10.66
B	.380	.420	9.65	10.66
C	.300	.320	7.62	8.12
φD	.139	.147	3.531	3.733
E	.560	.625	14.230	15.870
F	.100	.120	2.54	3.04
G	.040	.060	1.02	1.52
H	.500	.562	12.70	14.27
I		.250		6.35
J	.045	.060	1.14	1.52
K	.090	.110	2.29	2.79
L	.020	.040	.510	1.016
M	.190	.210	4.830	5.330
N	.175	.185	4.445	4.699
O	.030	.055	.762	1.390
P	.230	.270	5.850	6.850
Q	.015	.025	.380	.630
R	.080	.115	2.040	2.920

ZVN0106L/0108L/2110L

ABSOLUTE MAXIMUM RATINGS

	Parameters	ZVN0106L	ZVN0108L	ZVN2110L	Units
V_{DS}	Drain-source voltage	60	80	100	V
I_D	Continuous drain current (@ $T_A=25°C$)	0.46			A
I_D	Continuous drain current (@ $T_C=25°C$)	1.5			A
I_{DM}	Pulse drain current	6			A
V_{GS}	Gate-source voltage	±20			V
P_D	Max. power dissipation (@ $T_A=25°C$)	1.5			W
P_D	Max. power dissipation (@ $T_C=25°C$)	20			W
	Operating/Storage Temperature Range	−55 to +150			°C

ELECTRICAL CHARACTERISTICS (at T=25°C unless otherwise stated)

Parameter		Symbol	Min.	Typ.	Max.	Unit	Conditions
Drain-source breakdown voltage	ZVN0106L	BV_{DSS}	60	-	-	V	$I_D=1mA$, $V_{GS}=0$
	ZVN0108L		80	-	-		
	ZVN2110L		100	-	-		
Gate-source threshold voltage		$V_{GS(th)}$	0.8	-	2.4	V	$I_D=1mA$, $V_{DS}=V_{GS}$
Gate-body leakage		I_{GSS}	-	0.1	20	nA	$V_{GS}=\pm20V$, $V_{DS}=0$
Zero gate voltage Drain current (Note 2)		I_{DSS}	-	-	1	μA	V_{DS}=max. rating, $V_{GS}=0$
			-	-	100	μA	$V_{DS}=0.8 \times$ max. rating $V_{GS}=0$ (T=125°C)
On-state drain current*		$I_{D(ON)}$	1.5	2	-	A	$V_{DS}=25V$, $V_{GS}=10V$
Static drain-source ON-resistance*		$R_{DS(ON)}$	-	-	4	Ω	$I_D=1A$, $V_{GS}=10V$
Forward transconductance* (Note 2)		g_{fs}	0.25	0.35	-	S	$V_{DS}=25V$, $I_D=1A$
Input capacitance (Note 2)		C_{iss}	-	59	75	pF	$V_{DS}=25V$, $V_{GS}=0$, f=1MHz
Common source output capacitance (Note 2)		C_{oss}	-	16	25		
Reverse transfer capacitance (Note 2)		C_{rss}	-	4	8		
Turn-ON delay time (Notes 1 & 2)		$t_{d(on)}$	-	4	7	n secs	$V_{DD}=25V$, $I_D=1A$
Rise time (Notes 1 & 2)		t_r	-	4	8		
Turn-OFF delay time (Notes 1 & 2)		$t_{d(off)}$	-	8	13		
Fall time (Notes 1 & 2)		t_f	-	8	13		

*Measured under pulsed conditions. Width=300μs. Duty cycle ≤2%.

Note 1 Switching times measured with 50 ohm source impedance and <5ns rise time on a pulse generator.

Note 2 Sample test.

DRAIN-SOURCE DIODE CHARACTERISTICS

Parameter	Symbol	Typ.	Unit	Conditions
Forward ON voltage*	V_{SD}	0.97	V	$V_{GS}=0$, $I_S=1.5A$
Reverse recovery time	t_{rr}	215	n secs	$V_{GS}=0$, $I_F=1.5A$, $I_R=1A$

Reverse Recovery Test Circuit

Circuit for Measuring Switching Times

Switching Waveforms

Note:
Power MOSFET switching times are essentially independent of operating temperature

Fig. 1 Output Characteristics

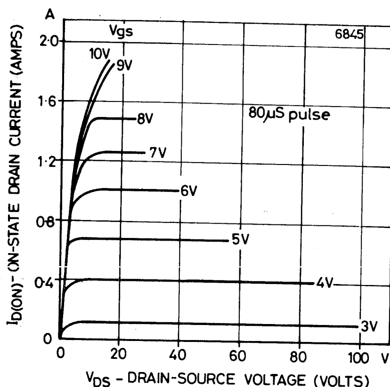


Fig. 2 Saturation Characteristics

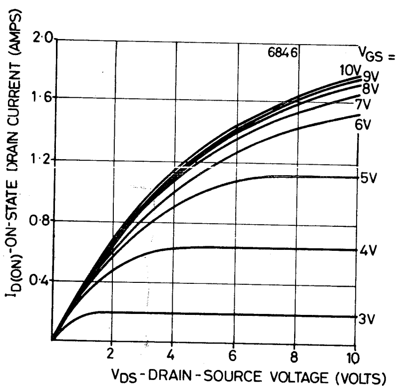


Fig. 3 Voltage Saturation Characteristics

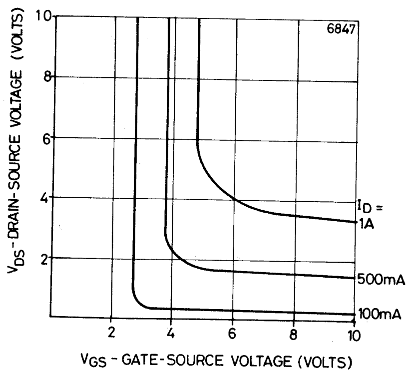


Fig. 4 Transfer Characteristics

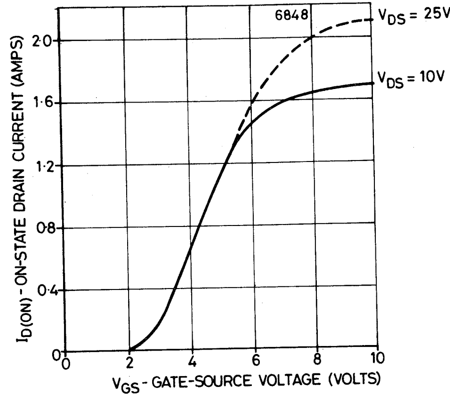


Fig. 5 Capacitance vs Drain-Source Voltage

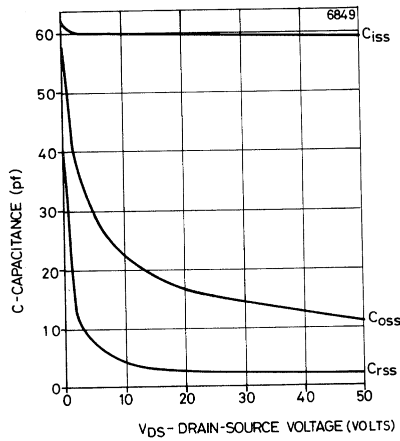
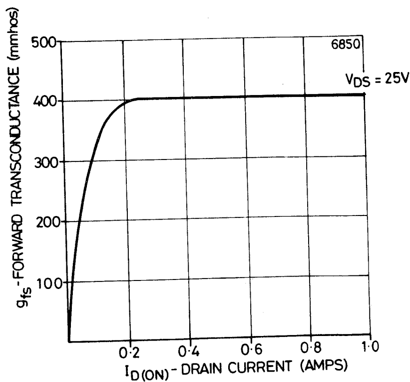


Fig. 6 Transconductance vs Drain Current



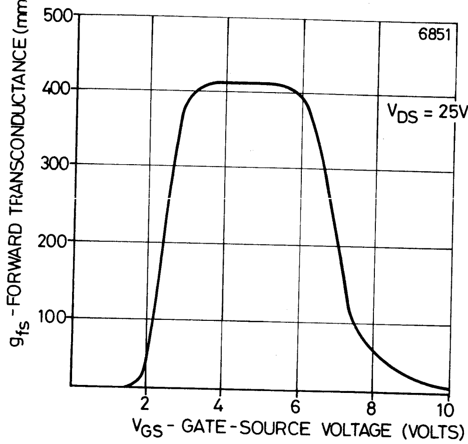


Fig. 7 Transconductance vs Gate-Source Voltage
6851
V_{DS} = 25V
g_{fs} - FORWARD TRANSCONDUCTANCE (mmhos)
500
400
300
200
100
2
4
6
8
10
V_{GS} - GATE-SOURCE VOLTAGE (VOLTS)

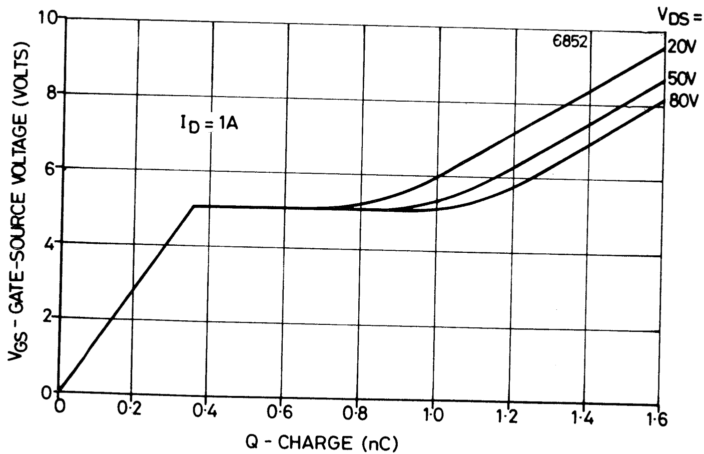


Fig. 8 Gate Charge vs Gate-Source Voltage
6852
V_{DS} =
20V
50V
80V
I_D = 1A
V_{GS} - GATE-SOURCE VOLTAGE (VOLTS)
10
8
6
4
2
0
0
0·2
0·4
0·6
0·8
1·0
1·2
1·4
1·6
Q - CHARGE (nC)

Fig. 9 ON-Resistance vs Gate-Source Voltage

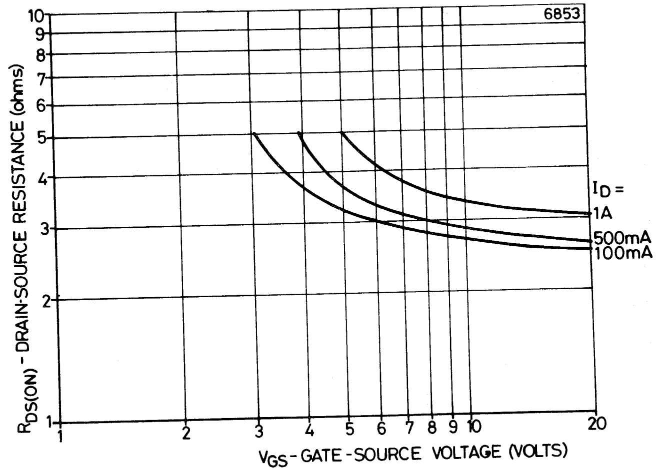
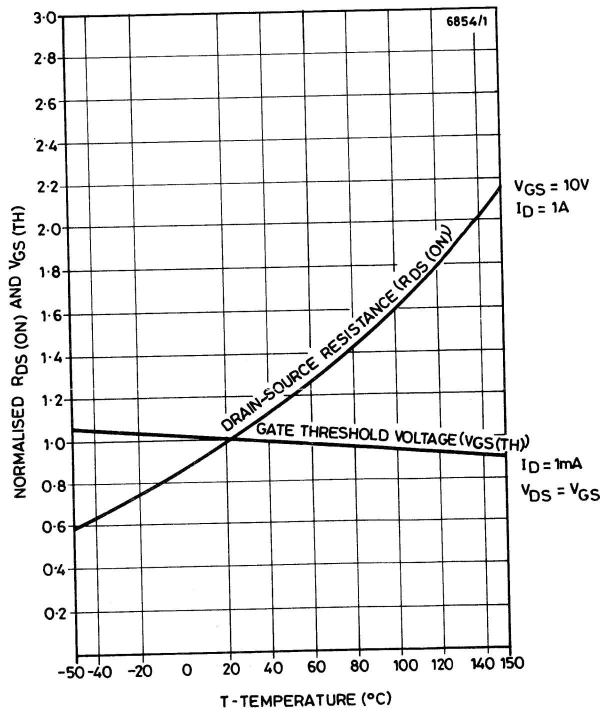


Fig. 10 Variation of $R_{DS(ON)}$ and $V_{GS(th)}$ with Temperature



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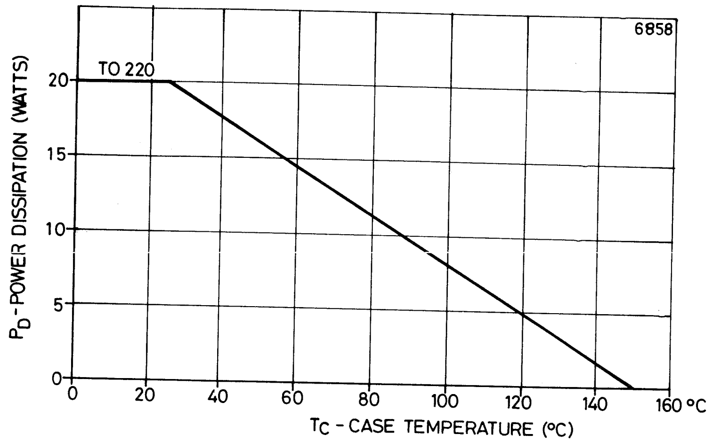

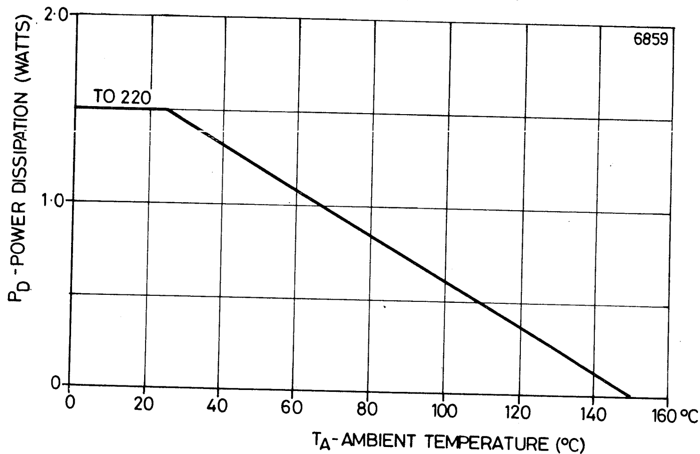

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Issue 2, April 1984 4.5M

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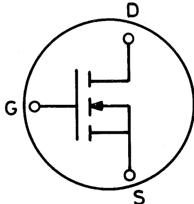
ZVN0117TA

N-Channel Enhancement-Mode Vertical DMOS Power FET

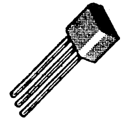
170V: 23 ohm: >100mA



N-Channel

FEATURES

- High Breakdown Voltage
- High Input Impedance
- High Speed Switching
- No Minority Storage Time
- CMOS Logic Compatible Input
- No Secondary Breakdown
- Excellent Temperature Stability
- Specially Suited for Telephone Subsets



PLASTIC E-LINE (TO-92)

DESCRIPTION

Compact geometries are the basis of the new generation of FERRANTI Power MOSFET transistors, optimised for low ON-resistance, low capacitances and fast switching speeds.

This particular device is specially designed for use in telephone switching circuits.

It is capable of withstanding simulated surges of lightning, to the circuit, of up to 1.5KV as laid down by British Telecom.

PRODUCT SUMMARY

BV_{DSS} 170V

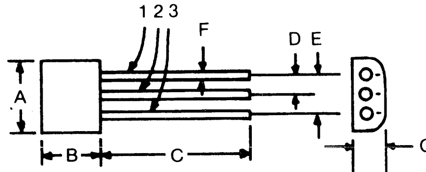
$I_{D(CONT)}$ 100mA

$R_{DS(ON)}$ 23Ω

P_D 700mW

Chip Size 0.042" × 0.042"

PACKAGE DIMENSIONS



PIN OUT	
1	Drain
2	Gate
3	Source

Also available with various lead bends and on Tape and Reel.

SYMBOL	INCHES		MILLIMETRES	
	MIN	MAX	MIN	MAX
A	.172	.188	4.37	4.77
B	.142	.158	3.61	4.01
C	.475	.525	12.06	13.34
D	.05		1.27	
E	.10		2.54	
F	.016	.019	.406	.495
G	.085	.095	2.16	2.42

ZVN0117TA

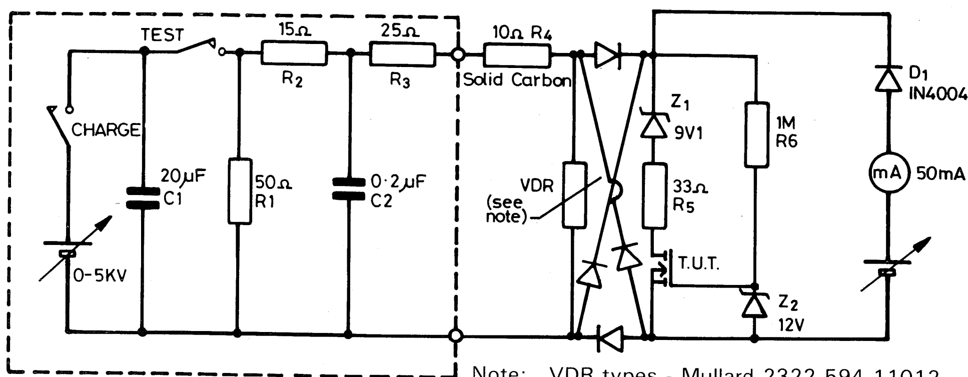
ABSOLUTE MAXIMUM RATINGS

Parameters	Symbol	Value	Units
Drain-source voltage	BV_{DSS}	170	V
Continuous drain current (@ $T_A=25°C$)	I_D	160	mA
Pulse drain current	I_{DM}	2	A
Gate-source voltage	V_{GS}	±20	V
Power dissipation (@ $T_A=25°C$)	P_D	0.7	W
Operating/Storage Temperature Range	T_j, T_{stg}	−55 to +150	°C

ELECTRICAL CHARACTERISTICS (at T=25°C unless otherwise stated)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Drain-source breakdown voltage	BV_{DSS}	170	-	-	V	$I_D=10\mu A$, $V_{GS}=0$
Gate-body leakage current	I_{GSS}	-	-	100	nA	$V_{GS}=\pm15V$, $V_{DS}=0$
Drain cut-off current	I_{DSS}	-	-	50	μA	$V_{GS}=0$, $V_{DS}=140V$
		(equiv. to 10μA @ 25°C)				$T_A=50°C$
On-state drain current	$I_{D(ON)}$	100	-	-	mA	$V_{GS}=3.3V$, $V_{DS}=3V$
Drain-source ON-resistance	$R_{DS(ON)}$	-	-	23	Ω	$V_{GS}=3.3V$, $I_D=100mA$
		-		23	Ω	$V_{GS}=3V$, $I_D=30mA$

SURGE TEST CIRCUIT FOR OUTPULSING FET



Note: VDR types - Mullard 2322 594 11012
Siemens S10V S07K 75
Matsushita ER2-C070K 10

6872

The transistor under test should withstand a surge applied via above circuit when C1 is charged to 1.5kV.

Fig. 1 Output Characteristics

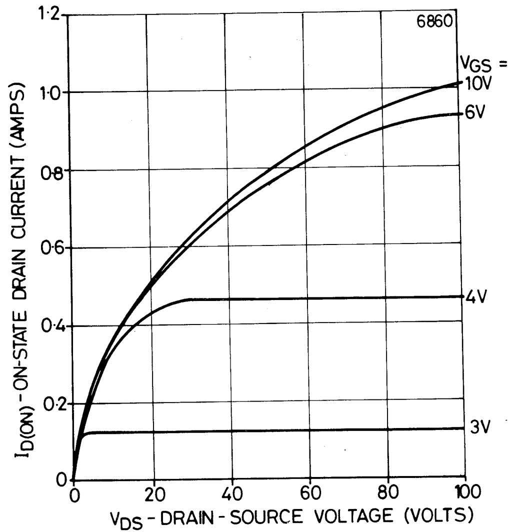
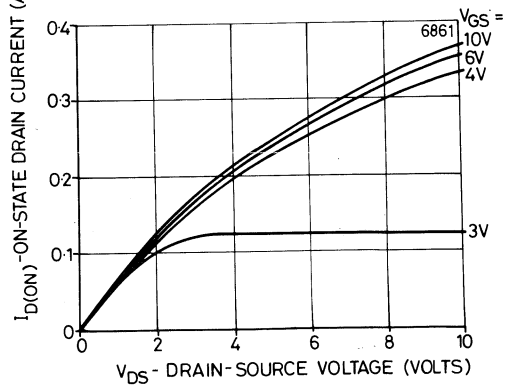


Fig. 2 Saturation Characteristics



ZVN0117TA

Fig. 3 Voltage Saturation Characteristics

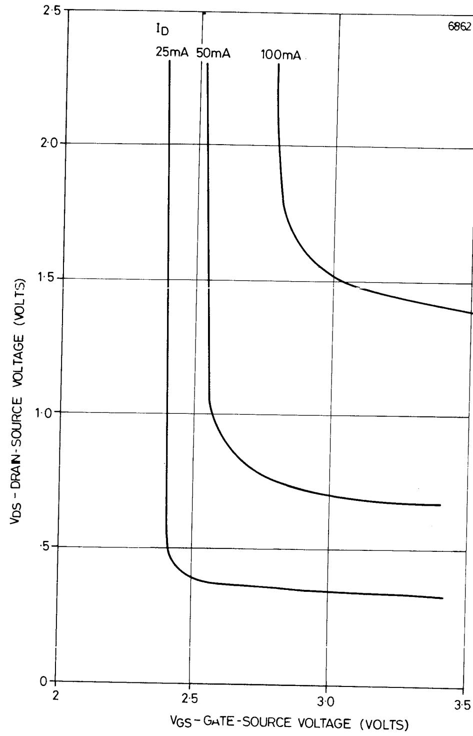


Fig. 4 Voltage Saturation Characteristics

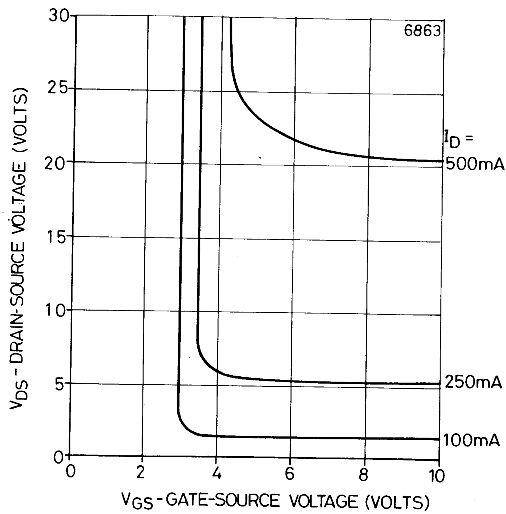


Fig. 5 Transfer Characteristics

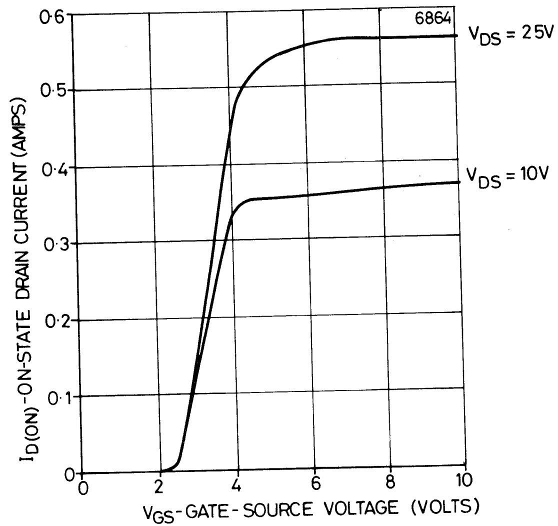


Fig. 6 Capacitance vs Drain-Source Voltage

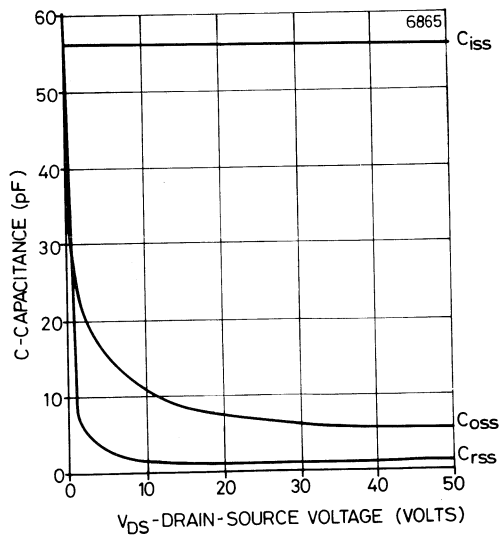


Fig. 7 Transconductance vs Drain Current

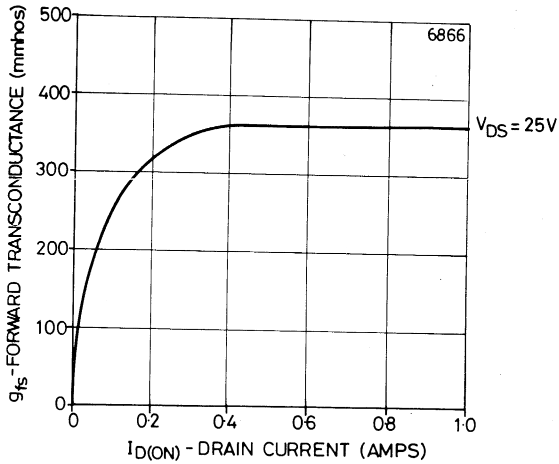


Fig. 8 Transconductance vs Gate-Source Voltage

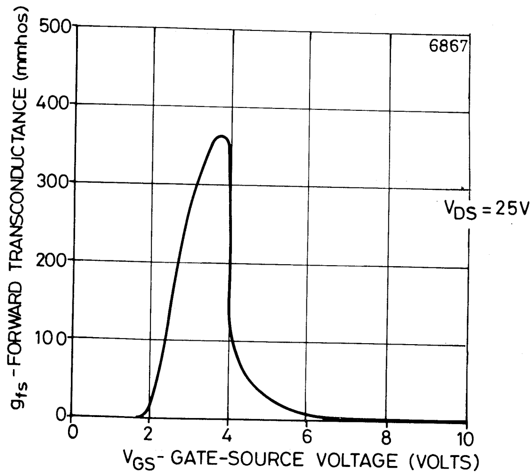


Fig. 9 Gate Charge vs Gate-Source Voltage

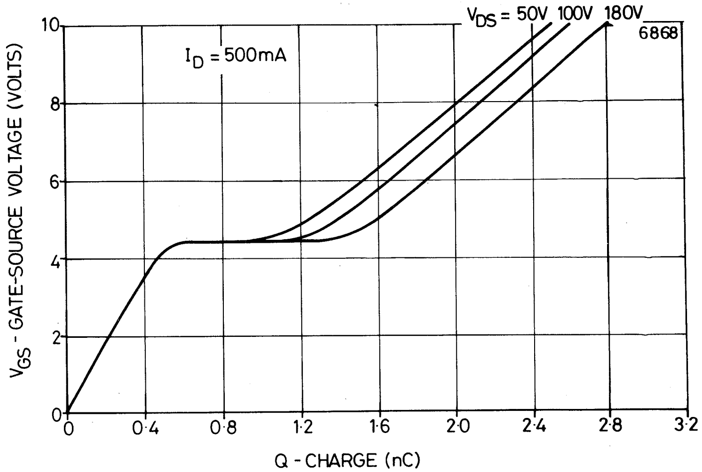
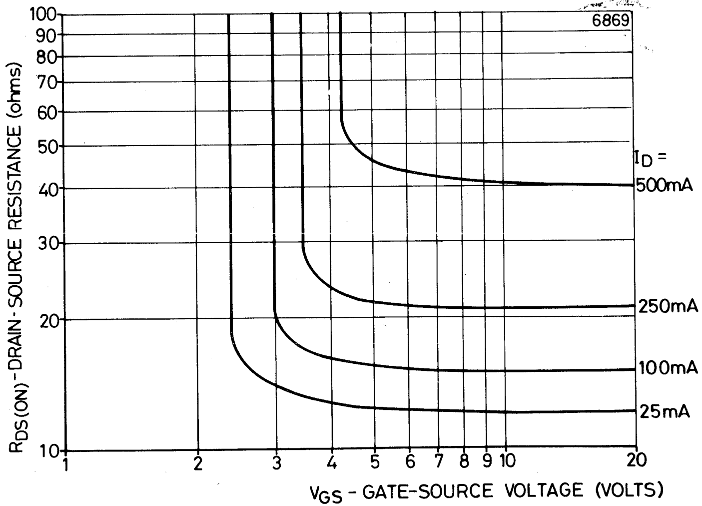


Fig. 10 ON-Resistance vs Gate-Source Voltage



ZVN0117TA

Fig. 11 Variation of $R_{DS(ON)}$ and $V_{GS(th)}$ with Temperature

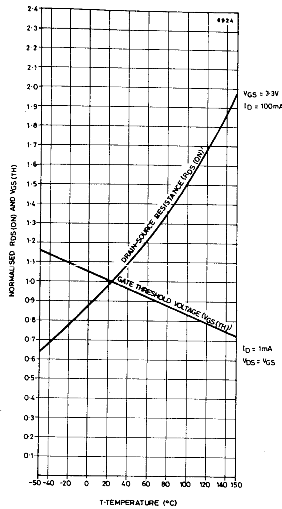
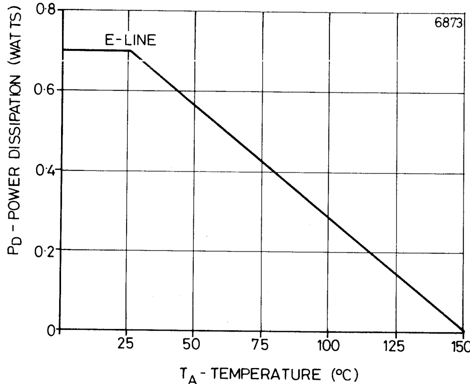


Fig. 12 Power Derating (Ambient)



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THE QUEEN'S AWARD FOR TECHNOLOGICAL ACHIEVEMENT

Issue 2, April 1984 4.5M

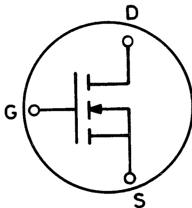
Printed in England CP

FERRANTI semiconductors ®

ZVN2115A
ZVN0120A

N-Channel Enhancement-Mode Vertical DMOS Power FET

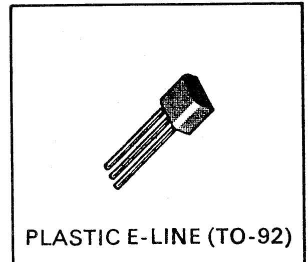
200V: 16 ohm: 0.16A



N-Channel

FEATURES

- Compact Geometry
- Fast Switching Speeds
- No Secondary Breakdown
- Excellent Temperature Stability
- High Input Impedance
- Low Current Drive
- Ease of Paralleling



PLASTIC E-LINE (TO-92)

DESCRIPTION

Compact OVERLAY (CELL) and INTER-DIGITATED geometries are the basis of the new generation of FERRANTI Power MOSFET transistors. These efficient geometries, optimised for low ON-resistance, low capacitances and fast switching speeds, with computer controlled processing combine to achieve greater device ruggedness.

The planar construction, coupled with ion implantation and the self-aligned poly-silicon gate manufacturing process, provides the reliability and stability in performance required in todays designs.

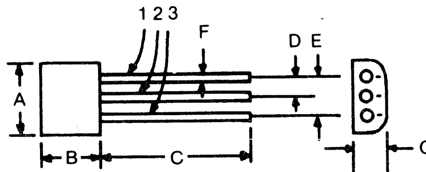
PRODUCT SUMMARY

Device Type	BV_{DSS}	$I_{D(CONT)}$	$R_{D(ON)}$
ZVN2115A	150V	0.16A	16Ω
ZVN0120A	200V	0.16A	16Ω

Chip Size 0.042″ × 0.042″

FERRANTI Power MOSFETS will directly interface with MICROPROCESSORS, LOGIC ARRAYS and standard IC LOGIC families including CMOS, TTL, PMOS and NMOS.

PACKAGE DIMENSIONS



PIN OUT	
1	Drain
2	Gate
3	Source

SYMBOL	INCHES		MILLIMETRES	
	MIN	MAX	MIN	MAX
A	.172	.188	4.37	4.77
B	.142	.158	3.61	4.01
C	.475	.525	12.06	13.34
D	.05		1.27	
E	.10		2.54	
F	.016	.019	.406	.495
G	.085	.095	2.16	2.42

Also available with various lead bends and on Tape and Reel.

ZVN2115A/0120A

ABSOLUTE MAXIMUM RATINGS

	Parameters	ZVN2115A	ZVN0120A	Units
V_{DS}	Drain-source voltage	150	200	V
I_D	Continuous drain current (@ $T_A = 25°C$)	0.16		A
I_D	Continuous drain current (@ $T_C = 25°C$)	-		A
I_{DM}	Pulse drain current	2		A
V_{GS}	Gate-source voltage	±20		V
P_D	Max. power dissipation (@ $T_A = 25°C$)	0.7		W
P_D	Max. power dissipation (@ $T_C = 25°C$)	-		W
	Operating/Storage Temperature Range	−55 to +150		°C

ELECTRICAL CHARACTERISTICS (at T=25°C unless otherwise stated)

Parameter		Symbol	Min.	Typ.	Max.	Unit	Conditions
Drain-source breakdown voltage	ZVN2115A	BV_{DSS}	150	-	-	V	$I_D = 1mA$
	ZVN0120A		200	-	-		$V_{GS} = 0$
Gate-source threshold voltage		$V_{GS(th)}$	1	-	3	V	$I_D = 1mA$, $V_{DS} = V_{GS}$
Gate-body leakage		I_{GSS}	-	0.1	20	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0$
Zero gate voltage Drain current (Note 2)		I_{DSS}	-	-	10	μA	V_{DS} = max. rating, $V_{GS} = 0$
			-	-	100	μA	$V_{DS} = 0.8 \times$ max. rating $V_{GS} = 0$ (T=125°C)
On-state drain current*		$I_{D(ON)}$	0.5	1	-	A	$V_{DS} = 25V$, $V_{GS} = 10V$
Static drain-source ON-resistance*		$R_{DS(ON)}$	-	-	16	Ω	$I_D = 0.25A$, $V_{GS} = 10V$
Forward transconductance* (Note 2)		g_{fs}	0.1	0.25	-	S	$V_{DS} = 25V$, $I_D = 0.25A$
Input capacitance (Note 2)		C_{iss}	-	62	85	pF	$V_{DS} = 25V$
Common source output capacitance (Note 2)		C_{oss}	-	9	20		$V_{GS} = 0$
Reverse transfer capacitance (Note 2)		C_{rss}	-	2	7		f=1MHz
Turn-ON delay time (Notes 1 & 2)		$t_{d(on)}$	-	3	7	n secs	$V_{DD} = 25V$
Rise time (Notes 1 & 2)		t_r	-	2	8		
Turn-OFF delay time (Notes 1 & 2)		$t_{d(off)}$	-	11	16		$I_D = 0.25A$
Fall time (Notes 1 & 2)		t_f	-	5	8		

*Measured under pulsed conditions. Width=300μs. Duty cycle ⩽2%.

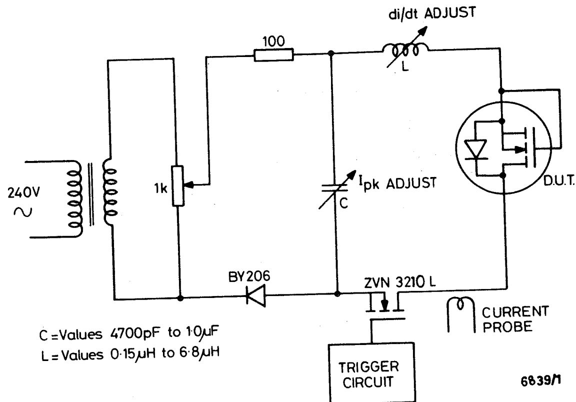
Note 1 Switching times measured with 50 ohm source impedance and <5ns rise time on a pulse generator.

Note 2 Sample test.

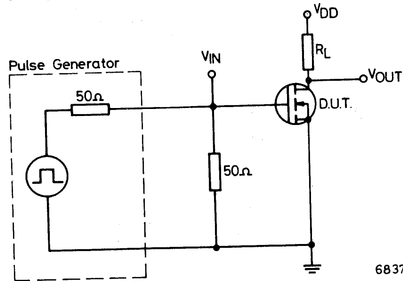
DRAIN-SOURCE DIODE CHARACTERISTICS

Parameter	Symbol	Typ.	Unit	Conditions
Forward ON voltage*	V_{SD}	0.76	V	$V_{GS}=0$, $I_S=160mA$
Reverse recovery time	t_{rr}	105	n secs	$V_{GS}=0$, $I_F=160mA$, $I_R=100mA$

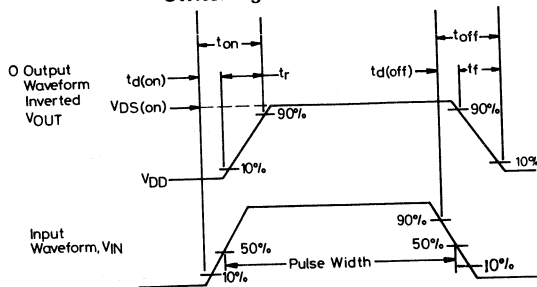
Reverse Recovery Test Circuit



Circuit for Measuring Switching Times



Switching Waveforms



Note:
Power MOSFET switching times are essentially independent of operating temperature

Fig. 1 Output Characteristics

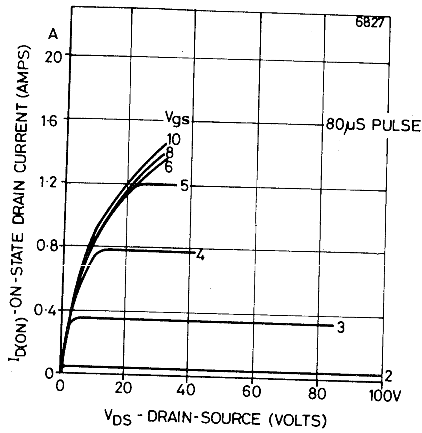


Fig. 2 Saturation Characteristics

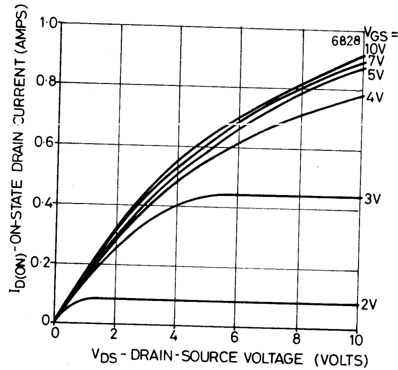


Fig. 3 Voltage Saturation Characteristics

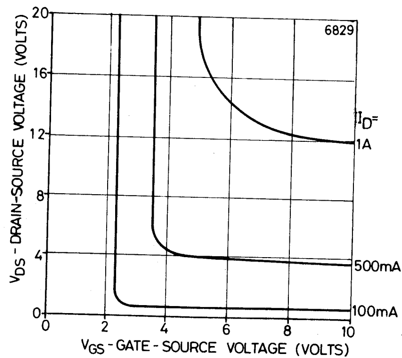


Fig. 4 Transfer Characteristics

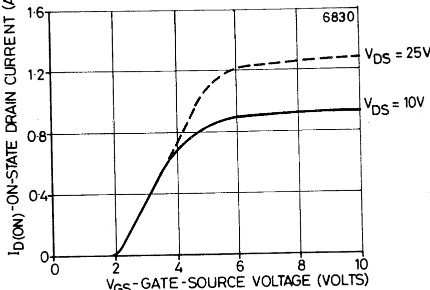


Fig. 5 Capacitance vs Drain-Source Voltage

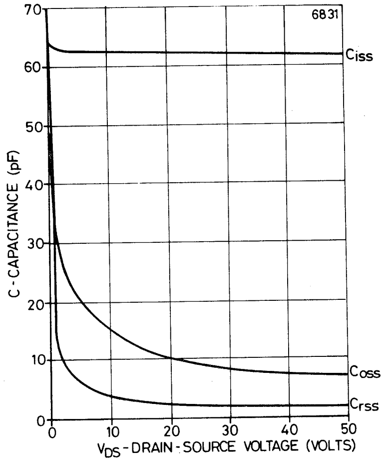


Fig. 6 Transconductance vs Drain Current

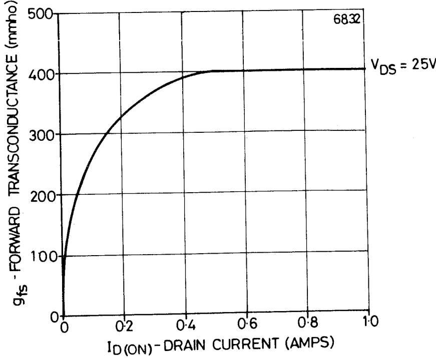


Fig. 7 Transconductance vs Gate-Source Voltage

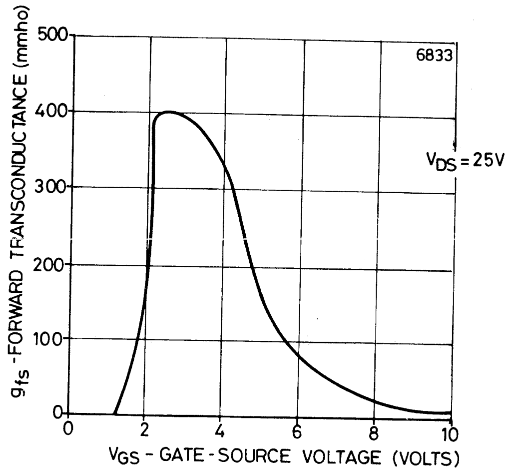


Fig. 8 Gate Charge vs Gate-Source Voltage

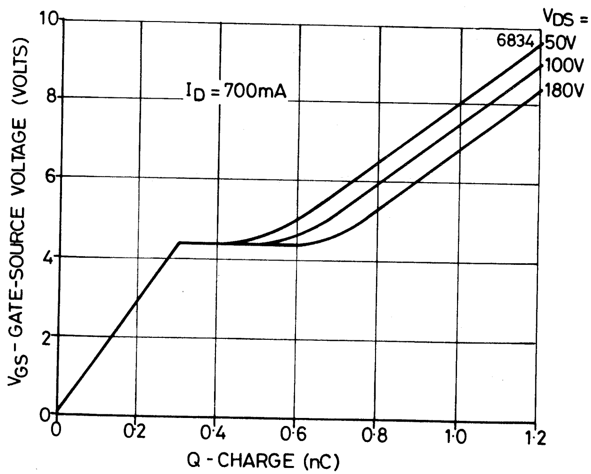


Fig. 9 ON-Resistance vs Gate-Source Voltage

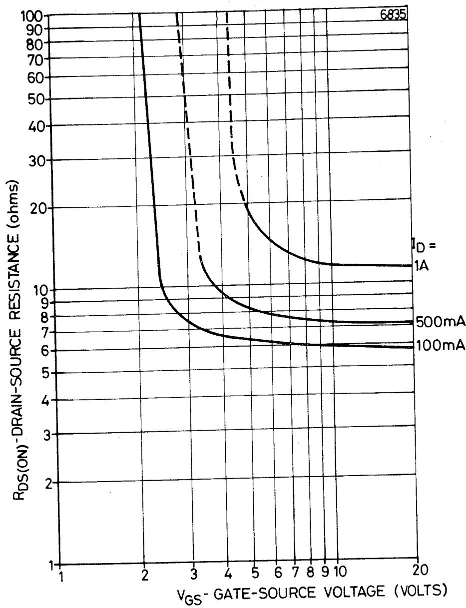


Fig. 10 Variation of $R_{DS(ON)}$ and $V_{GS(th)}$ with Temperature

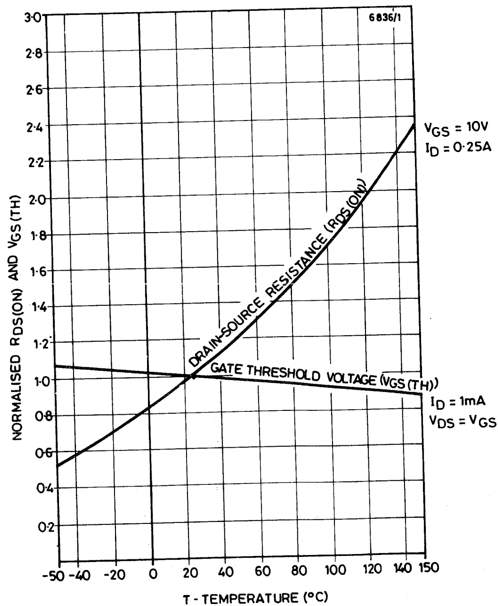
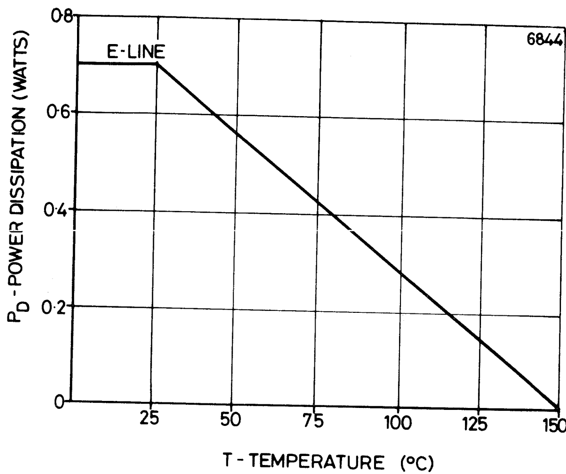


Fig. 11 Power Derating (Ambient)



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Issue 2, April 1984 4.5M

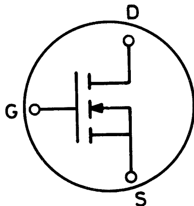
Printed in England CP

FERRANTI semiconductors®

ZVN2115B
ZVN0120B

N-Channel Enhancement-Mode Vertical DMOS Power FET

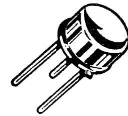
200V: 16 ohm: 0.42A



N-Channel

FEATURES

- Compact Geometry
- Fast Switching Speeds
- No Secondary Breakdown
- Excellent Temperature Stability
- High Input Impedance
- Low Current Drive
- Ease of Paralleling



TO-39 PACKAGE

DESCRIPTION

Compact OVERLAY (CELL) and INTER-DIGITATED geometries are the basis of the new generation of FERRANTI Power MOSFET transistors. These efficient geometries, optimised for low ON-resistance, low capacitances and fast switching speeds, with computer controlled processing combine to achieve greater device ruggedness.

The planar construction, coupled with ion implantation and the self-aligned poly-silicon gate manufacturing process, provides the reliability and stability in performance required in todays designs.

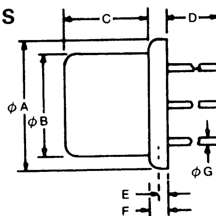
PRODUCT SUMMARY

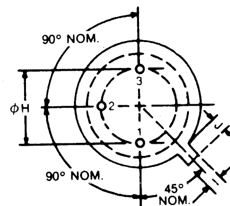
Device Type	BV_{DSS}	$I_{D(CONT)}$	$R_{D(ON)}$
ZVN2115B	150V	0.42A	16Ω
ZVN0120B	200V	0.42A	16Ω

Chip Size 0.042″ × 0.042″

FERRANTI Power MOSFETS will directly interface with MICROPROCESSORS, LOGIC ARRAYS and standard IC LOGIC families including CMOS, TTL, PMOS and NMOS.

PACKAGE DIMENSIONS





PIN OUT	
1	Source
2	Gate
3	Drain & Case

SYMBOL	INCHES		MILLIMETRES	
	MIN	MAX	MIN	MAX
φA	.350	.370	8.89	9.40
φB	.306	.335	7.77	8.51
C	.240	.260	6.10	6.60
D	.500		12.70	
E	.009	.023	.229	.584
F	.018	.045	.458	1.143
φG	.016	.021	.406	.533
φH	.190	.210	4.83	5.33
I	.028	.037	.711	.939
J	.026	.040	.660	1.016

ZVN2115B/0120B

ABSOLUTE MAXIMUM RATINGS

Parameters		ZVN2115B	ZVN0120B	Units
V_{DS}	Drain-source voltage	150	200	V
I_D	Continuous drain current (@ $T_A=25°C$)	0.16		A
I_D	Continuous drain current (@ $T_C=25°C$)	0.42		A
I_{DM}	Pulse drain current	2		A
V_{GS}	Gate-source voltage	±20		V
P_D	Max. power dissipation (@ $T_A=25°C$)	0.7		W
P_D	Max. power dissipation (@ $T_C=25°C$)	5		W
	Operating/Storage Temperature Range	−55 to +150		°C

ELECTRICAL CHARACTERISTICS (at T = 25°C unless otherwise stated)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Drain-source breakdown voltage ZVN2115B	BV_{DSS}	150	-	-	V	$I_D=1mA$, $V_{GS}=0$
Drain-source breakdown voltage ZVN0120B	BV_{DSS}	200	-	-	V	$I_D=1mA$, $V_{GS}=0$
Gate-source threshold voltage	$V_{GS(th)}$	1	-	3	V	$I_D=1mA$, $V_{DS}=V_{GS}$
Gate-body leakage	I_{GSS}	-	0.1	20	nA	$V_{GS}=\pm20V$, $V_{DS}=0$
Zero gate voltage Drain current (Note 2)	I_{DSS}	-	-	10	μA	V_{DS} = max. rating, $V_{GS}=0$
		-	-	100	μA	$V_{DS}=0.8\times$ max. rating $V_{GS}=0$ (T = 125°C)
On-state drain current*	$I_{D(ON)}$	0.5	1	-	A	$V_{DS}=25V$, $V_{GS}=10V$
Static drain-source ON-resistance*	$R_{DS(ON)}$	-	-	16	Ω	$I_D=0.25A$, $V_{GS}=10V$
Forward transconductance* (Note 2)	g_{fs}	0.1	0.25	-	S	$V_{DS}=25V$, $I_D=0.25A$
Input capacitance (Note 2)	C_{iss}	-	62	85	pF	$V_{DS}=25V$, $V_{GS}=0$, f = 1MHz
Common source output capacitance (Note 2)	C_{oss}	-	9	20	pF	
Reverse transfer capacitance (Note 2)	C_{rss}	-	2	7	pF	
Turn-ON delay time (Notes 1 & 2)	$t_{d(on)}$	-	3	7	n secs	$V_{DD}=25V$, $I_D=0.25A$
Rise time (Notes 1 & 2)	t_r	-	2	8	n secs	
Turn-OFF delay time (Notes 1 & 2)	$t_{d(off)}$	-	11	16	n secs	
Fall time (Notes 1 & 2)	t_f	-	5	8	n secs	

*Measured under pulsed conditions. Width = 300μs. Duty cycle ⩽ 2%.

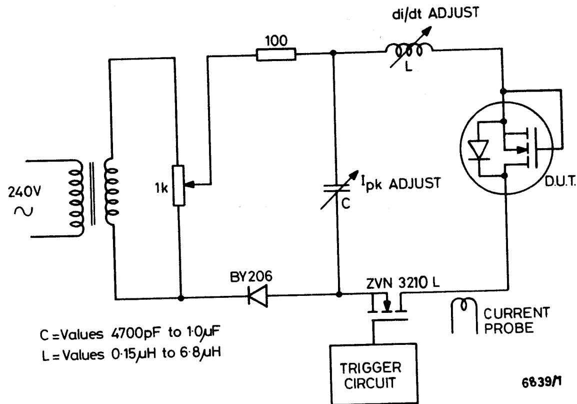
Note 1 Switching times measured with 50 ohm source impedance and <5ns rise time on a pulse generator.

Note 2 Sample test.

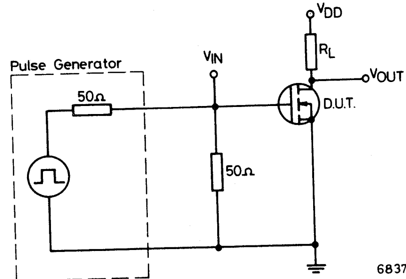
DRAIN-SOURCE DIODE CHARACTERISTICS

Parameter	Symbol	Typ.	Unit	Conditions
Forward ON voltage*	V_{SD}	0.70	V	$V_{GS}=0$, $I_S=420mA$
Reverse recovery time	t_{rr}	188	n secs	$V_{GS}=0$, $I_F=420mA$, $I_R=100mA$

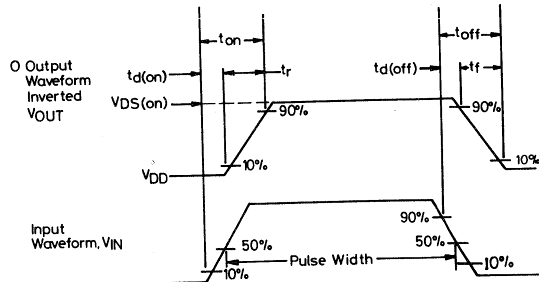
Reverse Recovery Test Circuit



Circuit for Measuring Switching Times



Switching Waveforms



Note:
Power MOSFET switching times are essentially independent of operating temperature

6838/1

Fig. 1 Output Characteristics

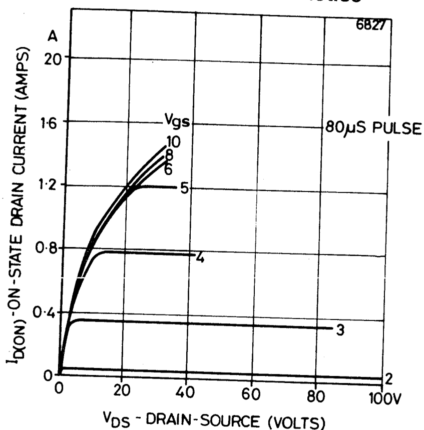


Fig. 2 Saturation Characteristics

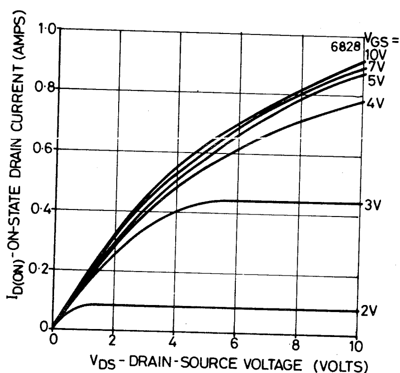


Fig. 3 Voltage Saturation Characteristics

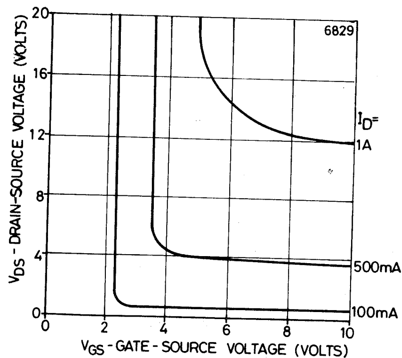


Fig. 4 Transfer Characteristics

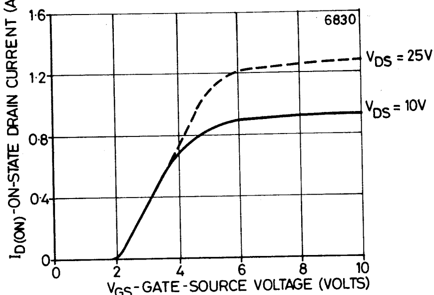


Fig. 5 Capacitance vs Drain-Source Voltage

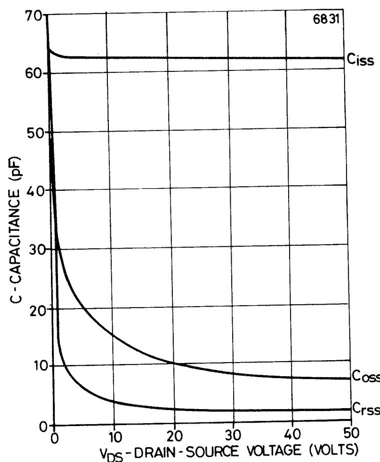


Fig. 6 Transconductance vs Drain Current

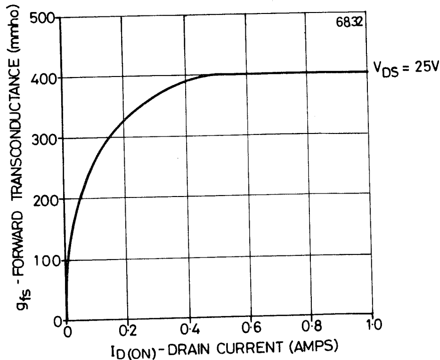


Fig. 7 Transconductance vs Gate-Source Voltage

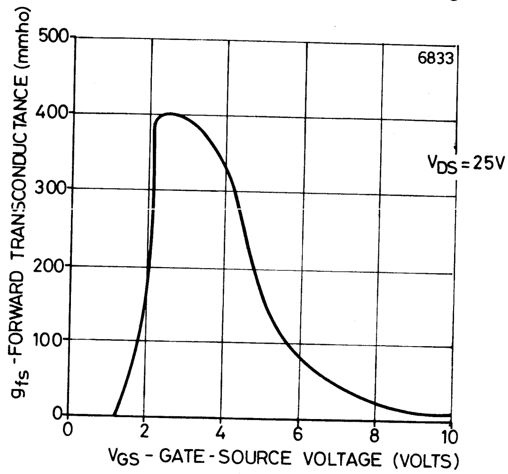


Fig. 8 Gate Charge vs Gate-Source Voltage

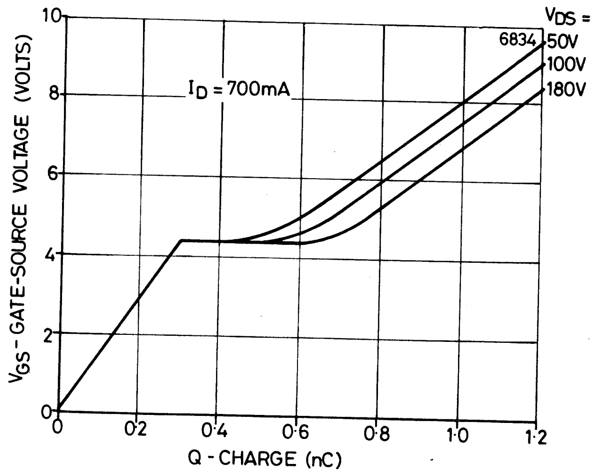


Fig. 9 ON-Resistance vs Gate-Source Voltage

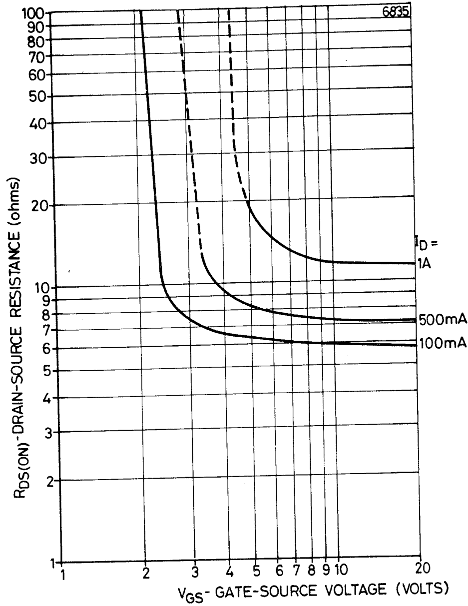
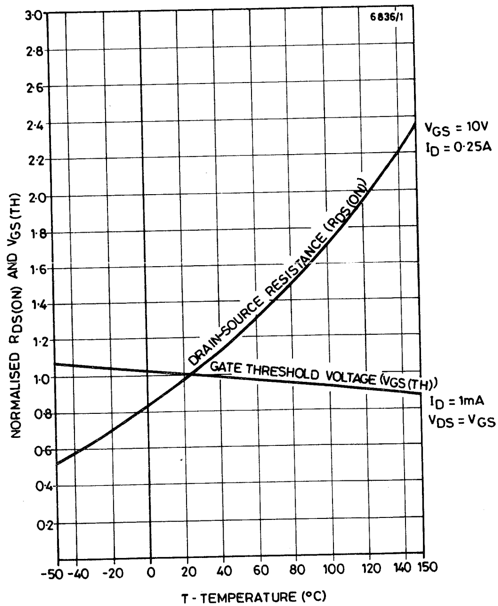


Fig. 10 Variation of $R_{DS(ON)}$ and $V_{GS(th)}$ with Temperature



ZVN2115B/0120B

Fig. 11 Power Derating (Case)

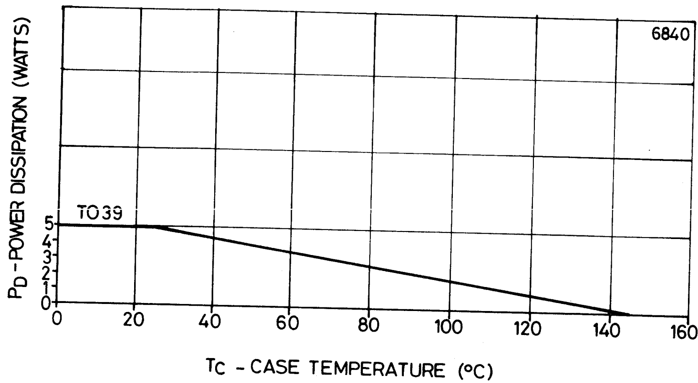
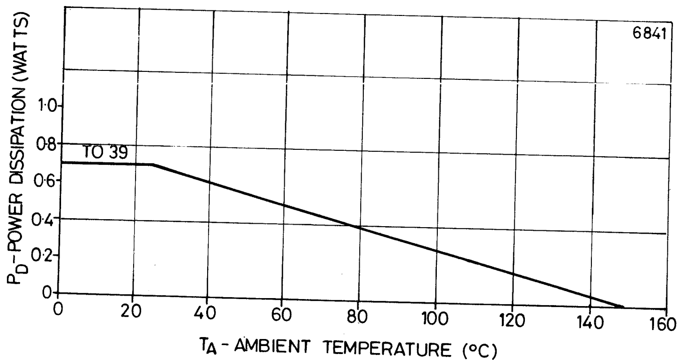


Fig. 12 Power Derating (Ambient)



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Gee Chang Hong Centre, Aberdeen, Hong Kong Tel: 5-538298-9 Telex: HX 74605

Issue 2, April 1984 4.5M

Printed in England CP

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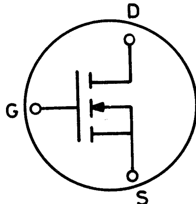
ZVN2115L
ZVN0120L

N-Channel Enhancement-Mode Vertical DMOS Power FET

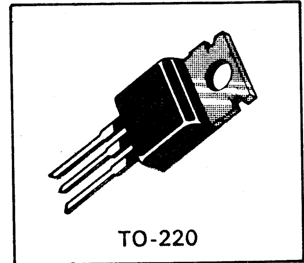
200V: 16 ohm: 0.5A



N-Channel

FEATURES

- Compact Geometry
- Fast Switching Speeds
- No Secondary Breakdown
- Excellent Temperature Stability
- High Input Impedance
- Low Current Drive
- Ease of Paralleling



TO-220

DESCRIPTION

Compact OVERLAY (CELL) and INTERDIGITATED geometries are the basis of the new generation of FERRANTI Power MOSFET transistors. These efficient geometries, optimised for low ON-resistance, low capacitances and fast switching speeds, with computer controlled processing combine to achieve greater device ruggedness.

The planar construction, coupled with ion implantation and the self-aligned poly-silicon gate manufacturing process, provides the reliability and stability in performance required in todays designs.

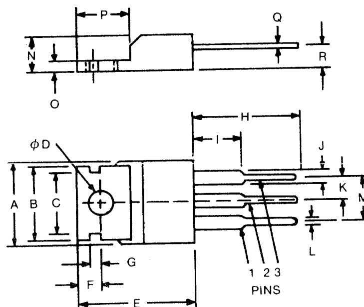
PRODUCT SUMMARY

Device Type	BV_{DSS}	$I_{D(CONT)}$	$R_{D(ON)}$
ZVN2115L	150V	0.5A	16Ω
ZVN0120L	200V	0.5A	16Ω

Chip Size 0.042″ × 0.042″

FERRANTI Power MOSFETS will directly interface with MICROPROCESSORS, LOGIC ARRAYS and standard IC LOGIC families including CMOS, TTL, PMOS and NMOS.

PACKAGE DIMENSIONS



PIN OUT	
1	Gate
2	Drain & Tab
3	Source

SYMBOL	INCHES		MILLIMETRES	
	MIN	MAX	MIN	MAX
A	.380	.420	9.65	10.66
B	.380	.420	9.65	10.66
C	.300	.320	7.62	8.12
φD	.139	.147	3.531	3.733
E	.560	.625	14.230	15.870
F	.100	.120	2.54	3.04
G	.040	.060	1.02	1.52
H	.500	.562	12.70	14.27
I		.250		6.35
J	.045	.060	1.14	1.52
K	.090	.110	2.29	2.79
L	.020	.040	.510	1.016
M	.190	.210	4.830	5.330
N	.175	.185	4.445	4.699
O	.030	.055	.762	1.390
P	.230	.270	5.850	6.850
Q	.015	.025	.380	.630
R	.080	.115	2.040	2.920

ZVN2115L/0120L

ABSOLUTE MAXIMUM RATINGS

	Parameters	ZVN2115L	ZVN0120L	Units
V_{DS}	Drain-source voltage	150	200	V
I_D	Continuous drain current (@ $T_A=25°C$)	0.23		A
I_D	Continuous drain current (@ $T_C=25°C$)	0.5		A
I_{DM}	Pulse drain current	2		A
V_{GS}	Gate-source voltage	±20		V
P_D	Max. power dissipation (@ $T_A=25°C$)	1.5		W
P_D	Max. power dissipation (@ $T_C=25°C$)	20		W
	Operating/Storage Temperature Range	−55 to +150		°C

ELECTRICAL CHARACTERISTICS (at T=25°C unless otherwise stated)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Drain-source breakdown voltage ZVN2115L	BV_{DSS}	150	-	-	V	$I_D=1mA$ $V_{GS}=0$
Drain-source breakdown voltage ZVN0120L		200	-	-		
Gate-source threshold voltage	$V_{GS(th)}$	1	-	3	V	$I_D=1mA$, $V_{DS}=V_{GS}$
Gate-body leakage	I_{GSS}	-	0.1	20	nA	$V_{GS}=\pm20V$, $V_{DS}=0$
Zero gate voltage Drain current (Note 2)	I_{DSS}	-	-	10	μA	V_{DS}=max. rating, $V_{GS}=0$
		-	-	100	μA	$V_{DS}=0.8\times$ max. rating $V_{GS}=0$ (T=125°C)
On-state drain current*	$I_{D(ON)}$	0.5	1	-	A	$V_{DS}=25V$, $V_{GS}=10V$
Static drain-source ON-resistance*	$R_{DS(ON)}$	-	-	16	Ω	$I_D=0.25A$, $V_{GS}=10V$
Forward transconductance* (Note 2)	g_{fs}	0.1	0.25	-	S	$V_{DS}=25V$, $I_D=0.25A$
Input capacitance (Note 2)	C_{iss}	-	62	85	pF	$V_{DS}=25V$
Common source output capacitance (Note 2)	C_{oss}	-	9	20		$V_{GS}=0$
Reverse transfer capacitance (Note 2)	C_{rss}	-	2	7		f=1MHz
Turn-ON delay time (Notes 1 & 2)	$t_{d(on)}$	-	3	7	n secs	$V_{DD}=25V$
Rise time (Notes 1 & 2)	t_r	-	2	8		
Turn-OFF delay time (Notes 1 & 2)	$t_{d(off)}$	-	11	16		$I_D=0.25A$
Fall time (Notes 1 & 2)	t_f	-	5	8		

*Measured under pulsed conditions. Width=300μs. Duty cycle ≤2%.

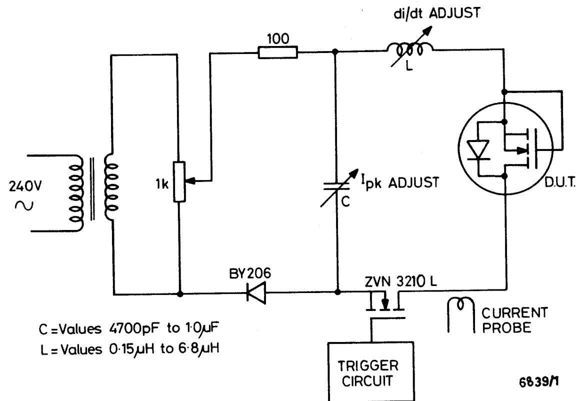
Note 1 Switching times measured with 50 ohm source impedance and <5ns rise time on a pulse generator.

Note 2 Sample test.

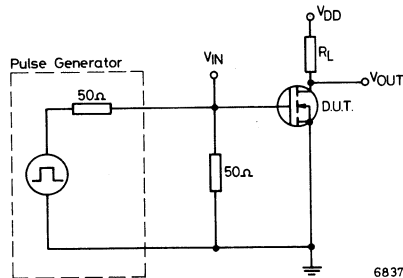
DRAIN-SOURCE DIODE CHARACTERISTICS

Parameter	Symbol	Typ.	Unit	Conditions
Forward ON voltage*	V_{SD}	0.96	V	$V_{GS}=0$, $I_S=0.5A$
Reverse recovery time	t_{rr}	50	n secs	$V_{GS}=0$, $I_F=0.5A$, $I_R=100mA$

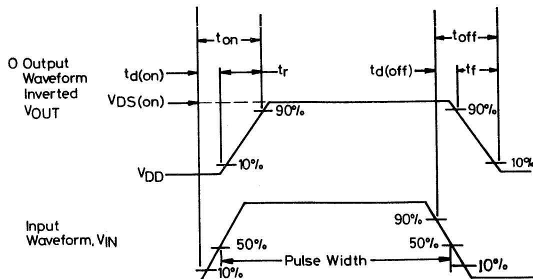
Reverse Recovery Test Circuit



Circuit for Measuring Switching Times



Switching Waveforms



Note:
Power MOSFET switching times are essentially independent of operating temperature

6838/1

Fig. 1 Output Characteristics

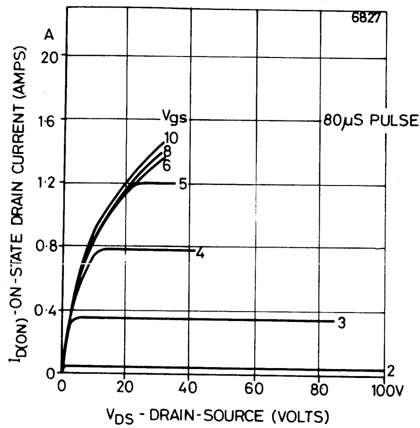


Fig. 2 Saturation Characteristics

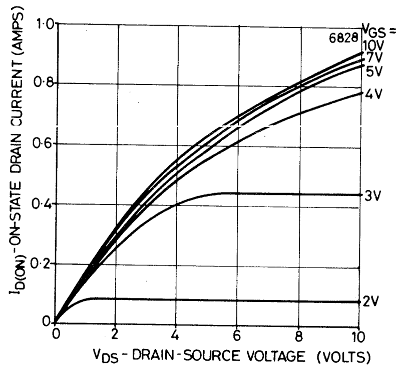


Fig. 3 Voltage Saturation Characteristics

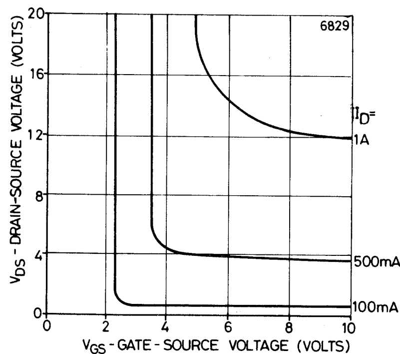


Fig. 4 Transfer Characteristics

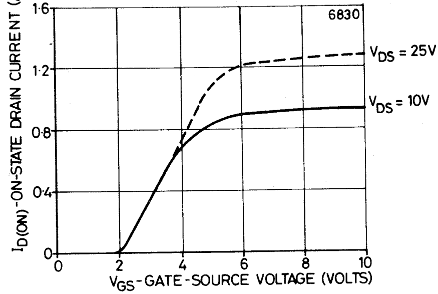


Fig. 5 Capacitance vs Drain-Source Voltage

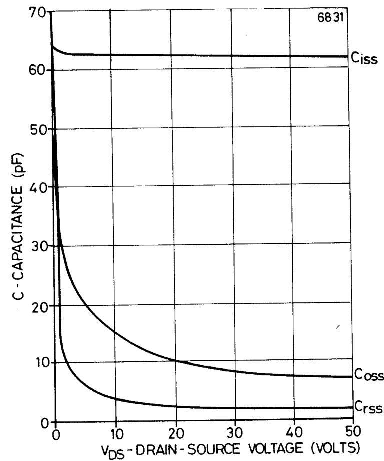


Fig. 6 Transconductance vs Drain Current

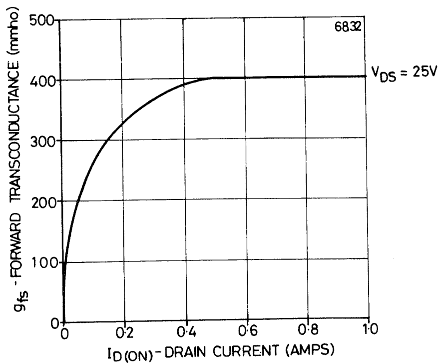


Fig. 7 Transconductance vs Gate-Source Voltage

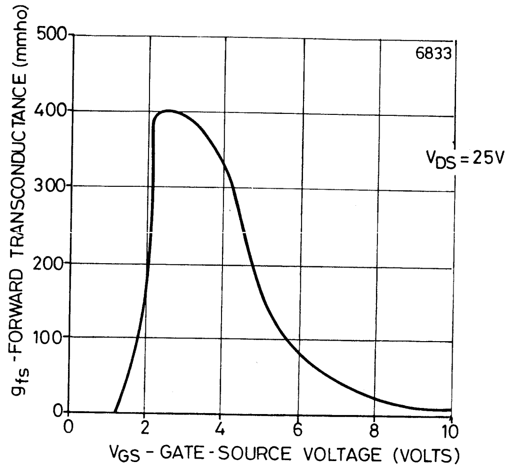


Fig. 8 Gate Charge vs Gate-Source Voltage

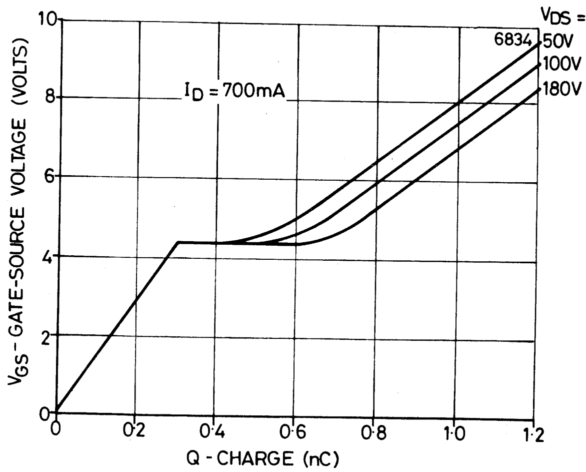


Fig. 9 ON-Resistance vs Gate-Source Voltage

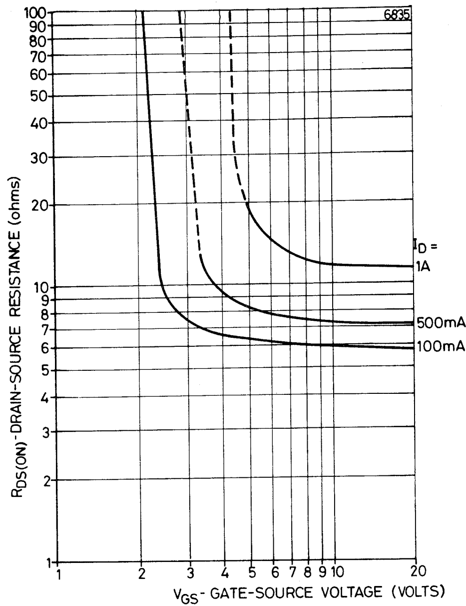
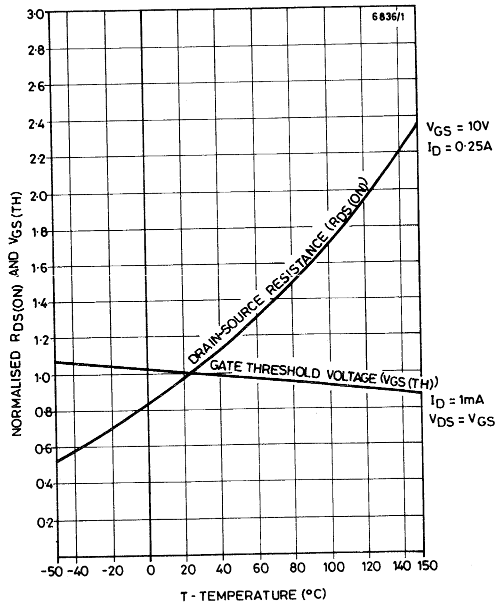


Fig. 10 Variation of $R_{DS(ON)}$ and $V_{GS(th)}$ with Temperature



ZVN2115L/0120L

Fig. 11 Power Derating (Case)

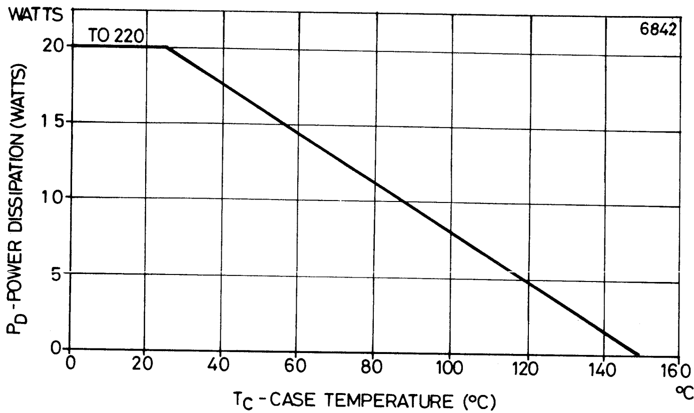
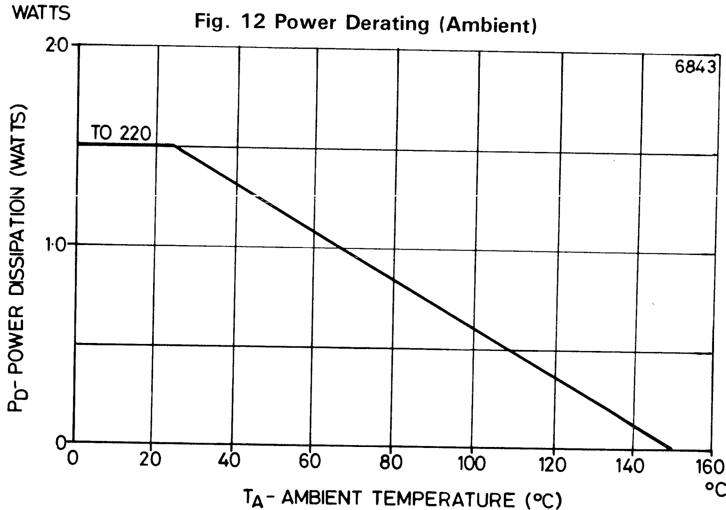


Fig. 12 Power Derating (Ambient)



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Tel: 408-438 2900 TWX: 910 598 4513
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Issue 2, April 1984 4.5M

Printed in England CP

Section 3

ZVN22 Range

ZVN2206B/L

ZVN2210B/L

ZVN2220B/L

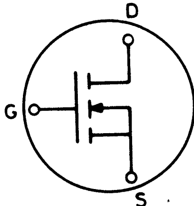
ZVN2224B/L

FERRANTI
semiconductors ®

ZVN2202B
ZVN2204B
ZVN2206B

N-Channel Enhancement-Mode Vertical DMOS Power FET

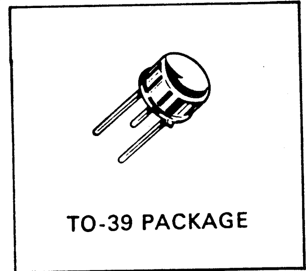
60V: 0.5 ohm: 4.8A



N-Channel

FEATURES

- Compact Geometry
- Fast Switching Speeds
- No Secondary Breakdown
- Excellent Temperature Stability
- High Input Impedance
- Low Current Drive
- Ease of Paralleling



TO-39 PACKAGE

DESCRIPTION

Compact OVERLAY (CELL) and INTER-DIGITATED geometries are the basis of the new generation of FERRANTI Power MOSFET transistors. These efficient geometries, optimised for low ON-resistance, low capacitances and fast switching speeds, with computer controlled processing combine to achieve greater device ruggedness.

The planar construction, coupled with ion implantation and the self-aligned poly-silicon gate manufacturing process, provides the reliability and stability in performance required in todays designs.

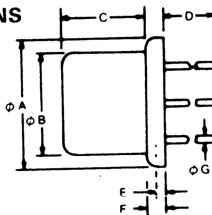
PRODUCT SUMMARY

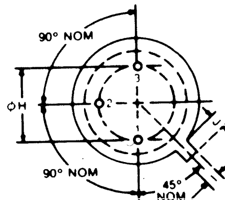
Device Type	BV_{DSS}	$I_{D(CONT)}$	$R_{D(ON)}$
ZVN2202B	20V	4.8A	0.5Ω
ZVN2204B	40V	4.8A	0.5Ω
ZVN2206B	60V	4.8A	0.5Ω

Chip Size 0.062″ × 0.072″

FERRANTI Power MOSFETS will directly interface with MICROPROCESSORS, LOGIC ARRAYS and standard IC LOGIC families including CMOS, TTL, PMOS and NMOS.

PACKAGE DIMENSIONS





SYMBOL	INCHES		MILLIMETRES	
	MIN	MAX	MIN	MAX
ØA	.350	.370	8.89	9.40
ØB	.306	.335	7.77	8.51
C	.240	.260	6.10	6.60
D	.500		12.70	
E	.009	.023	.229	.584
F	.018	.045	.458	1.143
ØG	.016	.021	.406	.533
ØH	.190	.210	4.83	5.33
I	.028	.037	.711	.939
J	.026	.040	.660	1.016

PIN OUT	
1	Source
2	Gate
3	Drain & Case

ZVN2202B/2204B/2206B

ABSOLUTE MAXIMUM RATINGS

	Parameters	ZVN2202B	ZVN2204B	ZVN2206B	Units
V_{DS}	Drain-source voltage	20	40	60	V
I_D	Continuous drain current (@ $T_A=25°C$)	0.9			A
I_D	Continuous drain current (@ $T_C=25°C$)	4.8			A
I_{DM}	Pulse drain current	16			A
V_{GS}	Gate-source voltage	± 20			V
P_D	Max. power dissipation (@ $T_A=25°C$)	0.7			W
P_D	Max. power dissipation (@ $T_C=25°C$)	20			W
	Operating/Storage Temperature Range	−55 to +150			°C

ELECTRICAL CHARACTERISTICS (at $T=25°C$ unless otherwise stated)

Parameter		Symbol	Min.	Typ.	Max.	Unit	Conditions
Drain source breakdown voltage	ZVN2202B	BV_{DSS}	20	-	-	V	$I_D=10\mu A$, $V_{GS}=0$
	ZVN2204B		40	-	-		
	ZVN2206B		60	-	-		
Gate-source threshold voltage		$V_{GS(th)}$	1	-	3	V	$I_D=2mA$, $V_{DS}=V_{GS}$
Gate body leakage		I_{GSS}	-	1	20	nA	$V_{GS}=\pm 20V$, $V_{DS}=0$
Zero gate voltage Drain current (Note 2)		I_{DSS}	-	-	2	μA	$V_{DS}=$ max. rating, $V_{GS}=0$
			-	-	0.2	mA	$V_{DS}=0.8 \times$ max. rating $V_{GS}=0$ ($T=125°C$)
On-state drain current*		$I_{D(ON)}$	4	8	-	A	$V_{DS}=18V$, $V_{GS}=10V$
Static drain-source ON-resistance*		$R_{DS(ON)}$	-	-	0.5	Ω	$I_D=2A$, $V_{GS}=10V$
Forward transconductance* (Note 2)		g_{fs}	-	1.4	-	S	$V_{DS}=18V$, $I_D=2A$
Input capacitance (Note 2)		C_{iss}	-	170	220	pF	$V_{DS}=18V$, $V_{GS}=0$, $f=1MHz$
Common source output capacitance (Note 2)		C_{oss}	-	80	100		
Reverse transfer capacitance (Note 2)		C_{rss}	-	35	80		
Turn-ON delay time (Notes 1 & 2)		$t_{d(on)}$	-	3.7	5	n secs	$V_{DD}=18V$, $I_D=2A$
Rise time (Notes 1 & 2)		t_r	-	14	20		
Turn-OFF delay time (Notes 1 & 2)		$t_{d(off)}$	-	17	26		
Fall time (Notes 1 & 2)		t_f	-	18	25		

*Measured under pulsed conditions. Width $=300\mu s$. Duty cycle $\leqslant 2\%$.

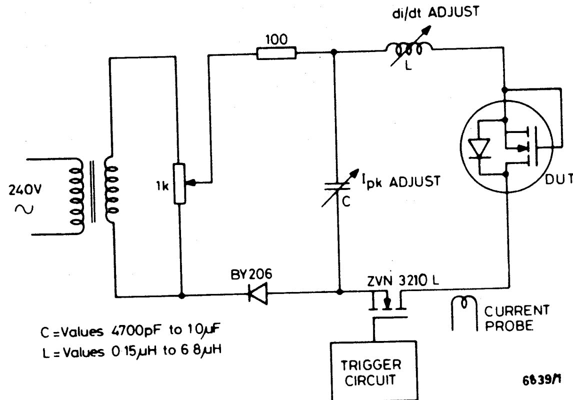
Note 1 Switching times measured with 50 ohm source impedance and $<5ns$ rise time on a pulse generator.

Note 2 Sample test.

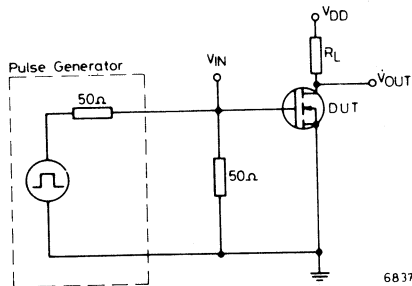
DRAIN-SOURCE DIODE CHARACTERISTICS

Parameter	Symbol	Typ.	Unit	Conditions
Forward ON voltage	V_{SD}	0.92	V	$V_{GS}=0$, $I_S=3.5A$
Reverse recovery time	t_{rr}	68	ns	$V_{GS}=0$, $I_F=3.5A$, $I_R=1.0A$

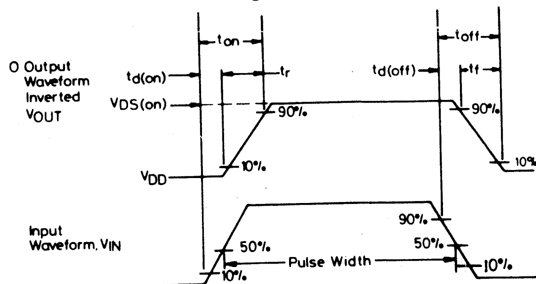
Reverse Recovery Test Circuit



Circuit for Measuring Switching Times



Switching Waveforms



Note
Power MOSFET switching times are essentially independent of operating temperature

ZVN2202B/2204B/2206B

Fig. 1 Output Characteristics

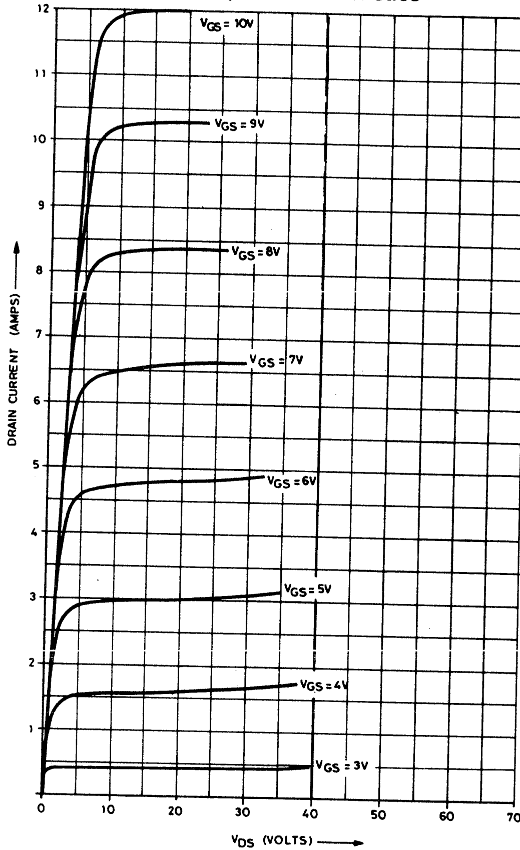


Fig. 2 Saturation Characteristics

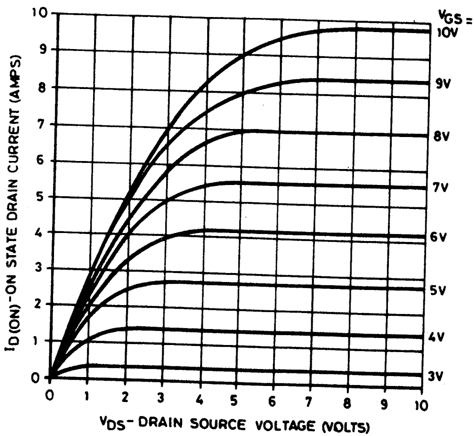


Fig. 3 Voltage Saturation Characteristics

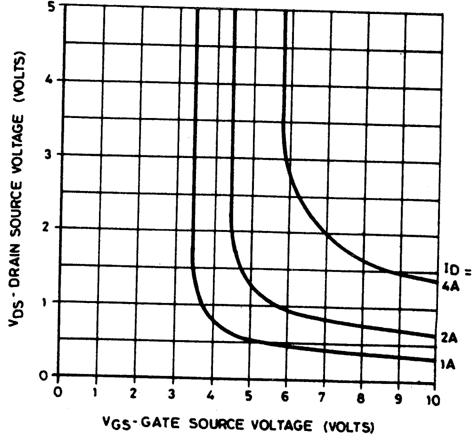


Fig. 4 Transfer Characteristics

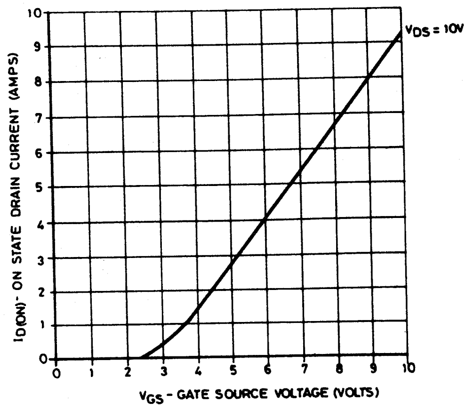


Fig. 5 Capacitance vs Drain-Source Voltage

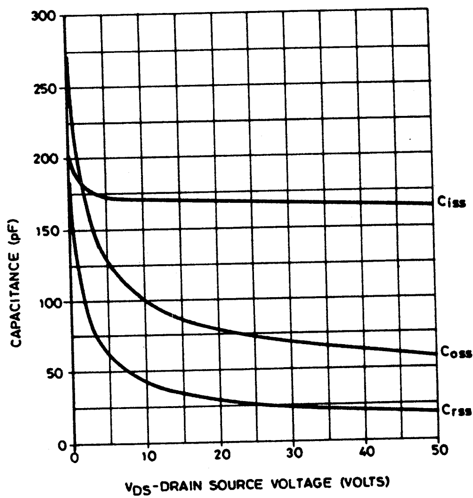
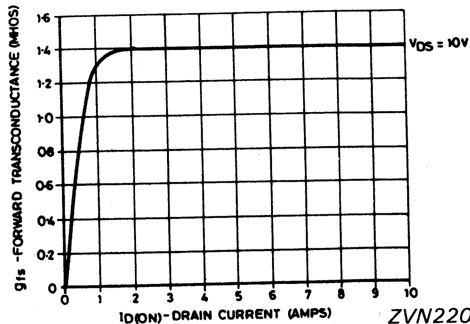


Fig. 6 Transconductance vs Drain-Current



ZVN2202B/2204B/2206B

Fig. 7 Transconductance vs Gate-Source Voltage

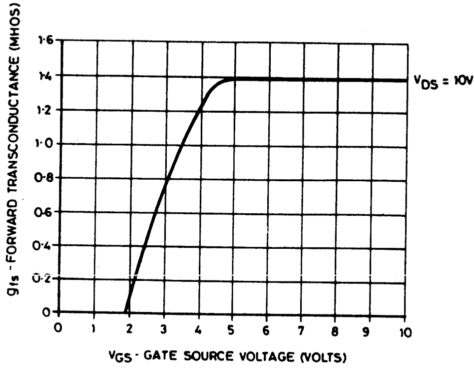


Fig. 8 Gate Charge vs Gate-Source Voltage

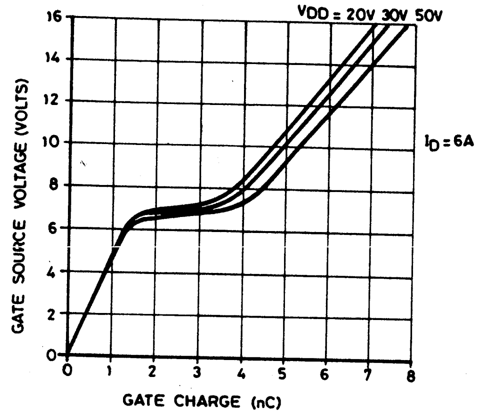


Fig. 9 ON-Resistance vs Gate-Source Voltage

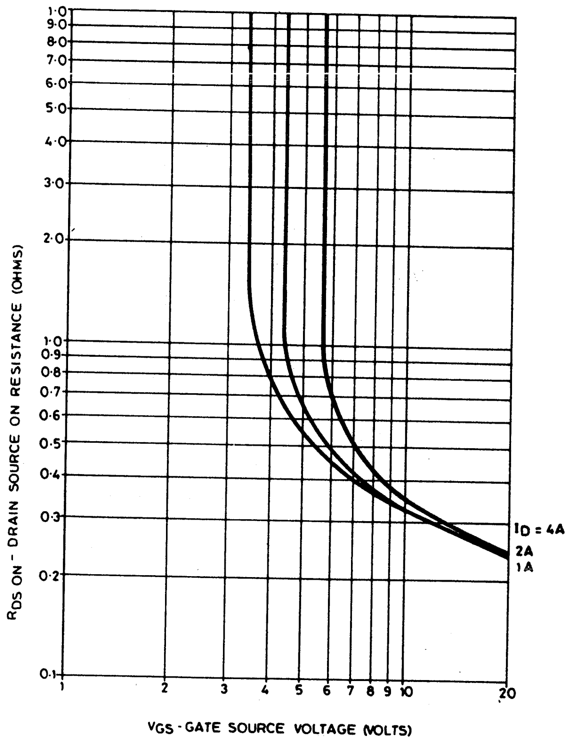
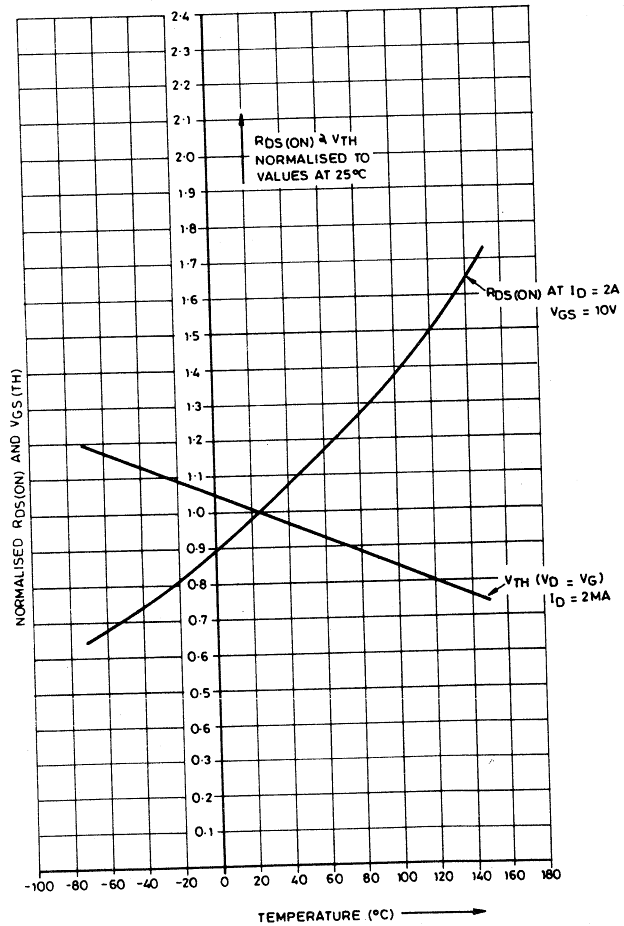


Fig. 10 Variation of $R_{DS(ON)}$ and $V_{GS(th)}$ with Temperature



ZVN2202B/2204B/2206B

Fig. 11 Power Derating (Case)

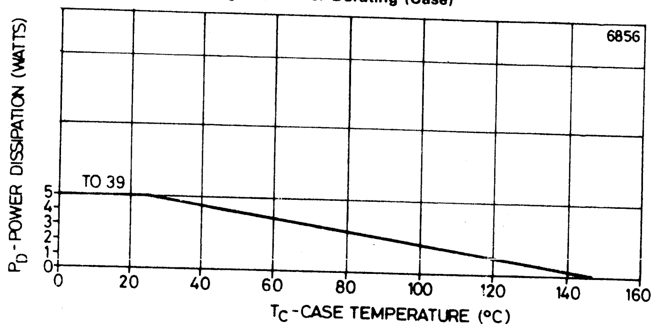
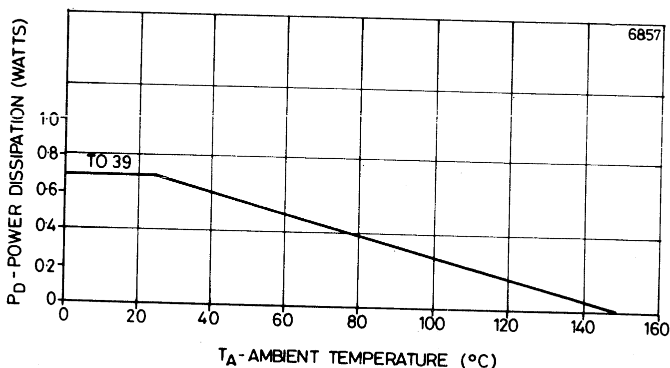


Fig. 12 Power Derating (Ambient)



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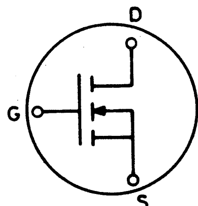
Issue 1, January 1985 5.1M

FERRANTI semiconductors®

ZVN2202L
ZVN2204L
ZVN2206L

N-Channel Enhancement-Mode Vertical DMOS Power FET

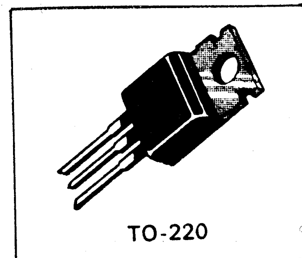
60V: 0.5 ohm: 4.8A



N-Channel

FEATURES

- Compact Geometry
- Fast Switching Speeds
- No Secondary Breakdown
- Excellent Temperature Stability
- High Input Impedance
- Low Current Drive
- Ease of Paralleling



TO-220

DESCRIPTION

Compact OVERLAY (CELL) and INTER-DIGITATED geometries are the basis of the new generation of FERRANTI Power MOSFET transistors. These efficient geometries, optimised for low ON-resistance, low capacitances and fast switching speeds, with computer controlled processing combine to achieve greater device ruggedness.

The planar construction, coupled with ion implantation and the self-aligned poly-silicon gate manufacturing process, provides the reliability and stability in performance required in todays designs.

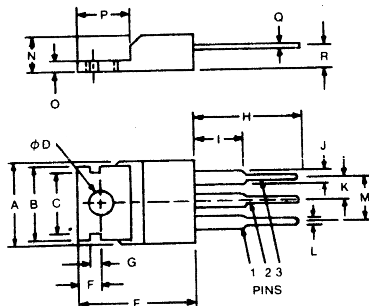
PRODUCT SUMMARY

Device Type	BV_{DSS}	$I_{D(CONT)}$	$R_{D(ON)}$
ZVN2202L	20V	4.8A	0.5Ω
ZVN2204L	40V	4.8A	0.5Ω
ZVN2206L	60V	4.8A	0.5Ω

Chip Size 0.062" × 0.072"

FERRANTI Power MOSFETS will directly interface with MICROPROCESSORS, LOGIC ARRAYS and standard IC LOGIC families including CMOS, TTL, PMOS and NMOS.

PACKAGE DIMENSIONS



PIN OUT	
1	Gate
2	Drain & Tab
3	Source

SYMBOL	INCHES		MILLIMETRES	
	MIN	MAX	MIN	MAX
A	.380	.420	9.65	10.66
B	.380	.420	9.65	10.66
C	.300	.320	7.62	8.12
ØD	.139	.147	3.531	3.733
E	.560	.625	14.230	15.870
F	.100	.120	2.54	3.04
G	.040	.060	1.02	1.52
H	.500	.562	12.70	14.27
I		.250		6.35
J	.045	.060	1.14	1.52
K	.090	.110	2.29	2.79
L	.020	.040	.510	1.016
M	.190	.210	4.830	5.330
N	.175	.185	4.445	4.699
O	.030	.055	.762	1.390
P	.230	.270	5.850	6.850
Q	.015	.025	.380	.630
R	.080	.115	2.040	2.920

ZVN2202L/2204L/2206L

ABSOLUTE MAXIMUM RATINGS

	Parameters	ZVN2202L	ZVN2204L	ZVN2206L	Units
V_{DS}	Drain-source voltage	20	40	60	V
I_D	Continuous drain current (@ $T_A = 25°C$)	1.3			A
I_D	Continuous drain current (@ $T_C = 25°C$)	4.8			A
I_{DM}	Pulse drain current	16			A
V_{GS}	Gate-source voltage	±20			V
P_D	Max. power dissipation (@ $T_A = 25°C$)	1.5			W
P_D	Max. power dissipation (@ $T_C = 25°C$)	20			W
	Operating/Storage Temperature Range	−55 to +150			°C

ELECTRICAL CHARACTERISTICS (at $T = 25°C$ unless otherwise stated)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Drain source breakdown voltage ZVN2202L	BV_{DSS}	20	-	-	V	$I_D = 10\mu A$, $V_{GS} = 0$
Drain source breakdown voltage ZVN2204L	BV_{DSS}	40	-	-	V	
Drain source breakdown voltage ZVN2206L	BV_{DSS}	60	-	-	V	
Gate-source threshold voltage	$V_{GS(th)}$	1	-	3	V	$I_D = 2mA$, $V_{DS} = V_{GS}$
Gate body leakage	I_{GSS}	-	1	20	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0$
Zero gate voltage Drain current (Note 2)	I_{DSS}	-	-	2	μA	V_{DS} = max. rating, $V_{GS} = 0$
		-	-	0.2	mA	$V_{DS} = 0.8 \times$ max. rating $V_{GS} = 0$ ($T = 125°C$)
On-state drain current*	$I_{D(ON)}$	4	8	-	A	$V_{DS} = 18V$, $V_{GS} = 10V$
Static drain-source ON-resistance*	$R_{DS(ON)}$	-	-	0.5	Ω	$I_D = 2A$, $V_{GS} = 10V$
Forward transconductance* (Note 2)	g_{fs}	-	1.4	-	S	$V_{DS} = 18V$, $I_D = 2A$
Input capacitance (Note 2)	C_{iss}	-	170	220	pF	$V_{DS} = 18V$ $V_{GS} = 0$ $f = 1MHz$
Common source output capacitance (Note 2)	C_{oss}	-	80	100	pF	
Reverse transfer capacitance (Note 2)	C_{rss}	-	35	80	pF	
Turn-ON delay time (Notes 1 & 2)	$t_{d(on)}$	-	3.7	5	n secs	$V_{DD} = 18V$ $I_D = 2A$
Rise time (Notes 1 & 2)	t_r	-	14	20	n secs	
Turn-OFF delay time (Notes 1 & 2)	$t_{d(off)}$	-	17	26	n secs	
Fall time (Notes 1 & 2)	t_f	-	18	25	n secs	

*Measured under pulsed conditions. Width = 300μs. Duty cycle ≤ 2%.

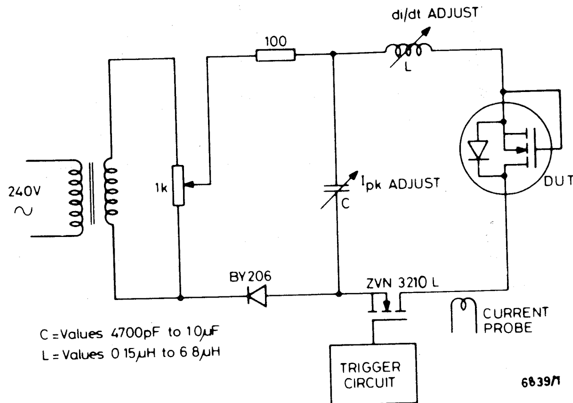
Note 1 Switching times measured with 50 ohm source impedance and <5ns rise time on a pulse generator.

Note 2 Sample test.

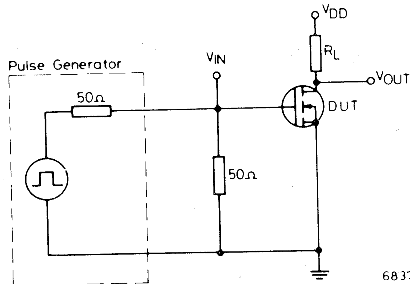
DRAIN-SOURCE DIODE CHARACTERISTICS

Parameter	Symbol	Typ.	Unit	Conditions
Forward ON voltage	V_{SD}	0.95	V	$V_{GS}=0$, $I_S=4A$
Reverse recovery time	t_{rr}	59	ns	$V_{GS}=0$, $I_F=4A$, $I_R=1A$

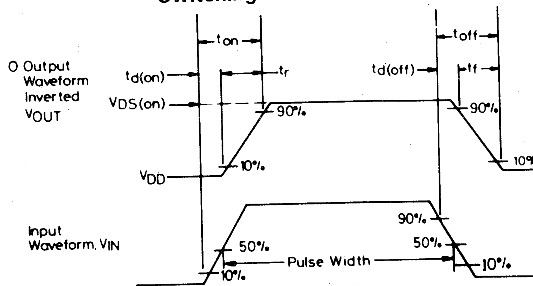
Reverse Recovery Test Circuit



Circuit for Measuring Switching Times

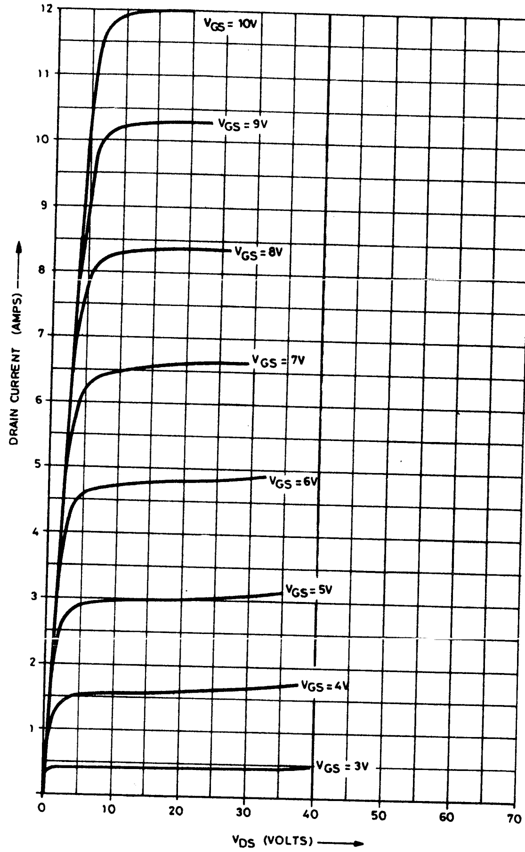


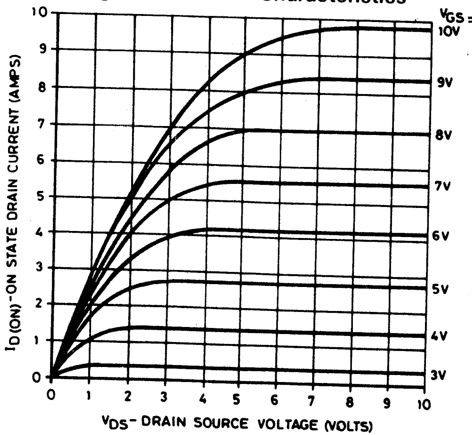
Switching Waveforms



Note
Power MOSFET switching times are essentially independent of operating temperature

ZVN2202L/2204L/2206L





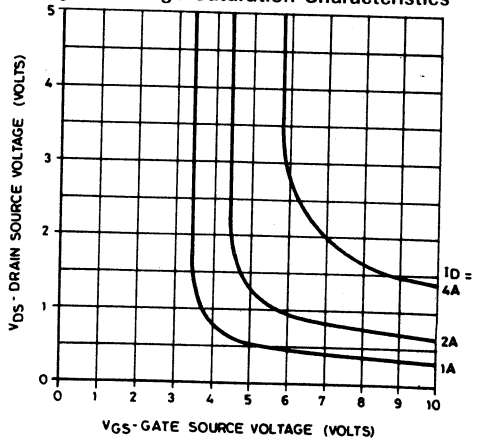


Fig. 4 Transfer Characteristics

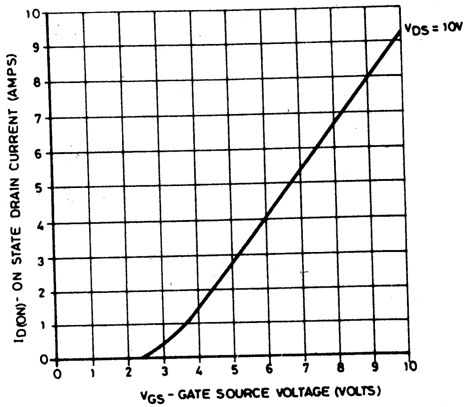


Fig. 5 Capacitance vs Drain-Source Voltage

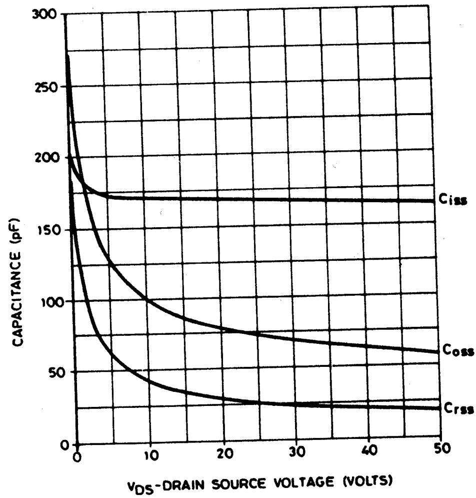
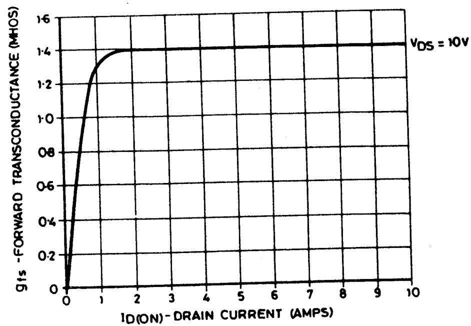


Fig. 6 Transconductance vs Drain-Current



ZVN2202L/2204L/2206L

Fig. 7

Transconductance vs Gate-Source Voltage

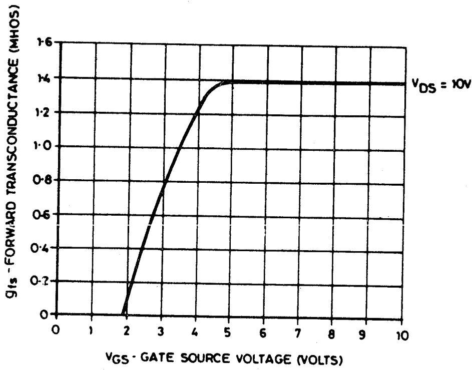


Fig. 8

Gate Charge vs Gate-Source Voltage

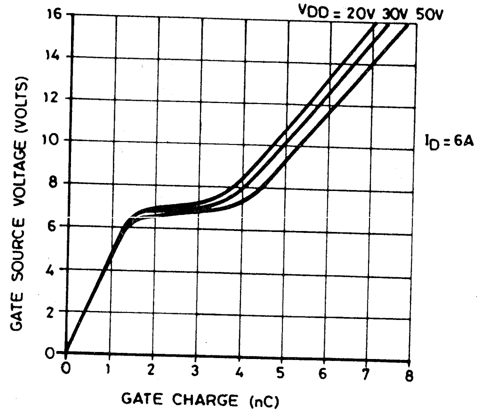


Fig. 9 ON-Resistance vs Gate-Source Voltage

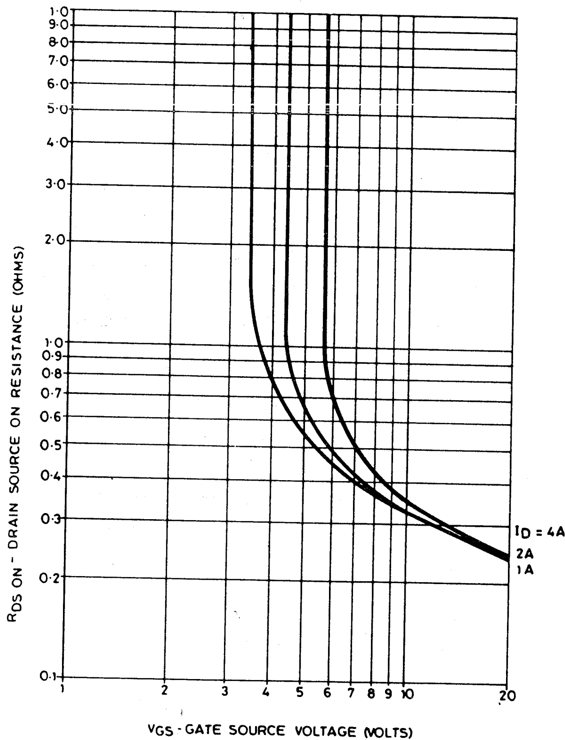


Fig. 10 Variation of $R_{DS(ON)}$ and $V_{GS(th)}$ with Temperature

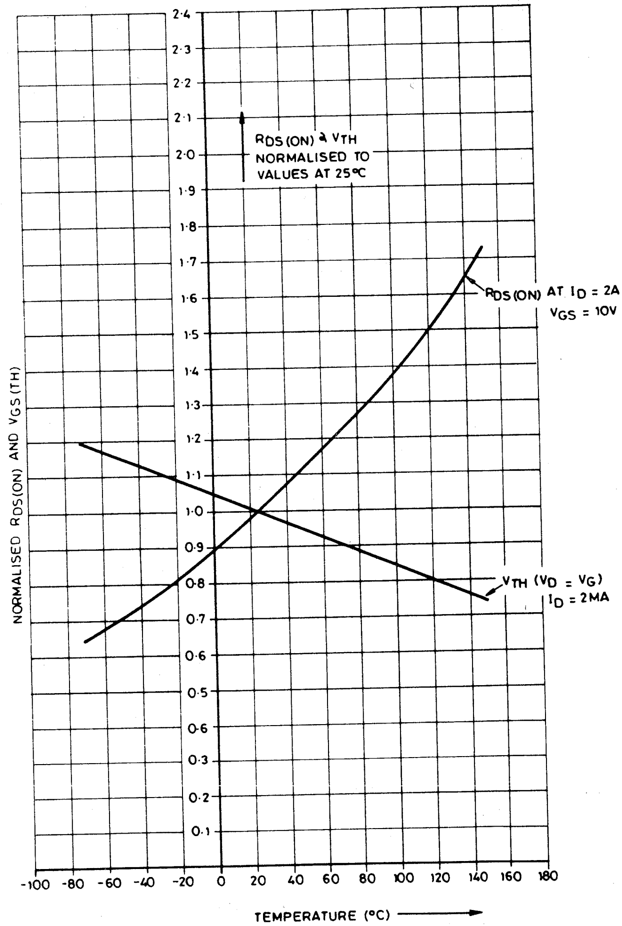


Fig. 11 Power Derating (Case)

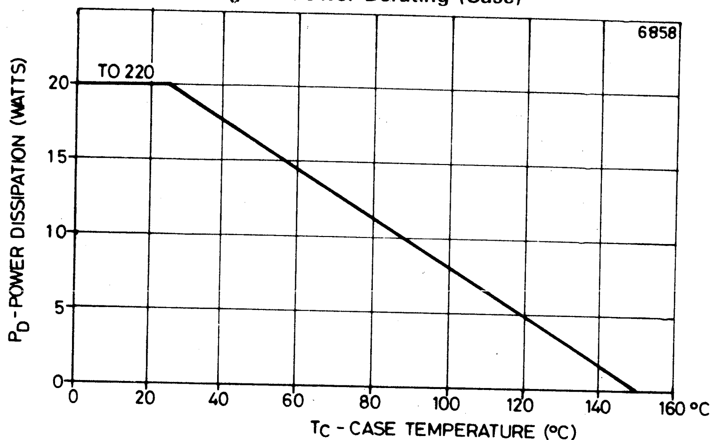
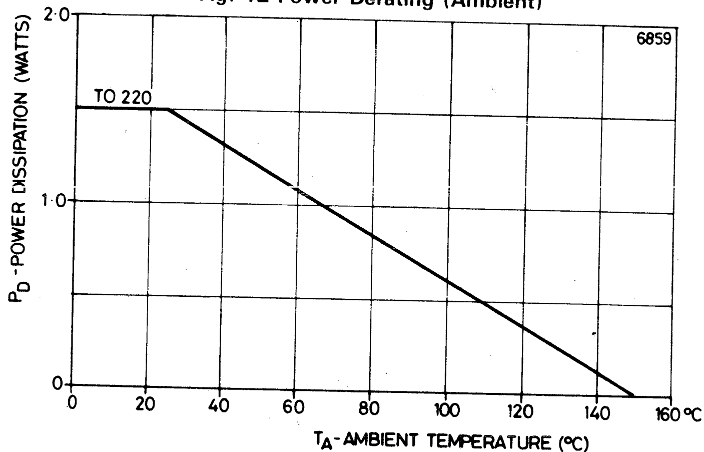


Fig. 12 Power Derating (Ambient)



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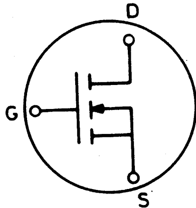
FERRANTI semiconductors®

ZVN2208B
ZVN2210B

N-Channel Enhancement-Mode Vertical DMOS Power FET

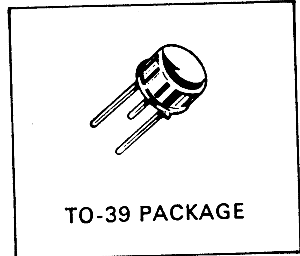
100V: 0.8 ohm: 3.45A



N-Channel

FEATURES

- Compact Geometry
- Fast Switching Speeds
- No Secondary Breakdown
- Excellent Temperature Stability
- High Input Impedance
- Low Current Drive
- Ease of Paralleling



TO-39 PACKAGE

DESCRIPTION

Compact OVERLAY (CELL) and INTER-DIGITATED geometries are the basis of the new generation of FERRANTI Power MOSFET transistors. These efficient geometries, optimised for low ON-resistance, low capacitances and fast switching speeds, with computer controlled processing combine to achieve greater device ruggedness.

The planar construction, coupled with ion implantation and the self-aligned poly-silicon gate manufacturing process, provides the reliability and stability in performance required in todays designs.

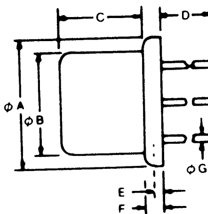
PRODUCT SUMMARY

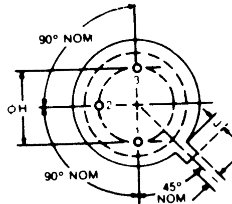
Device Type	BV_{DSS}	$I_{D(CONT)}$	$R_{D(ON)}$
ZVN2208B	80V	3.45A	0.8Ω
ZVN2210B	100V	3.45A	0.8Ω

Chip Size 0.062″ × 0.072″

FERRANTI Power MOSFETS will directly interface with MICROPROCESSORS, LOGIC ARRAYS and standard IC LOGIC families including CMOS, TTL, PMOS and NMOS.

PACKAGE DIMENSIONS





SYMBOL	INCHES		MILLIMETRES	
	MIN	MAX	MIN	MAX
ØA	.350	.370	8.89	9.40
ØB	.306	.335	7.77	8.51
C	.240	.260	6.10	6.60
D	.500		12.70	
E	.009	.023	.229	.584
F	.018	.045	.458	1.143
ØG	.016	.021	.406	.533
ØH	.190	.210	4.83	5.33
I	.028	.037	.711	.939
J	.026	.040	.660	1.016

PIN OUT	
1	Source
2	Gate
3	Drain & Case

ZVN2208B/2210B

ABSOLUTE MAXIMUM RATINGS

Parameters		ZVN2208B	ZVN2210B	Units
V_{DS}	Drain-source voltage	80	100	V
I_D	Continuous drain current (@ $T_A=25°C$)	0.65		A
I_D	Continuous drain current (@ $T_C=25°C$)	3.45		A
I_{DM}	Pulse drain current	12		A
V_{GS}	Gate-source voltage	± 20		V
P_D	Max. power dissipation (@ $T_A=25°C$)	0.7		W
P_D	Max. power dissipation (@ $T_C=25°C$)	20		W
	Operating/Storage Temperature Range	-55 to $+150$		°C

ELECTRICAL CHARACTERISTICS (at T = 25°C unless otherwise stated)

Parameter		Symbol	Min.	Typ.	Max.	Unit	Conditions
Drain source breakdown voltage	ZVN2208B	BV_{DSS}	80	-	-	V	$I_D=10\mu A$, $V_{GS}=0$
	ZVN2210B		100	-	-		
Gate-source threshold voltage		$V_{GS(th)}$	1	-	3	V	$I_D=2mA$, $V_{DS}=V_{GS}$
Gate body leakage		I_{GSS}	-	1	20	nA	$V_{GS}=\pm 20V$, $V_{DS}=0$
Zero gate voltage Drain current (Note 2)		I_{DSS}	-	-	2	μA	V_{DS} = max. rating, $V_{GS}=0$
			-	-	0.2	mA	$V_{DS}=0.8 \times$ max. rating $V_{GS}=0$ ($T=125°C$)
On-state drain current*		$I_{D(ON)}$	3	6	-	A	$V_{DS}=25V$, $V_{GS}=10V$
Static drain-source ON-resistance*		$R_{DS(ON)}$	-	-	0.8	Ω	$I_D=2A$, $V_{GS}=10V$
Forward transconductance* (Note 2)		g_{fs}	-	1.2	-	S	$V_{DS}=25V$, $I_D=1.5A$
Input capacitance (Note 2)		C_{iss}	-	160	220	pF	$V_{DS}=25V$, $V_{GS}=0$, $f=1MHz$
Common source output capacitance (Note 2)		C_{oss}	-	50	75	pF	
Reverse transfer capacitance (Note 2)		C_{rss}	-	16	25	pF	
Turn-ON delay time (Notes 1 & 2)		$t_{d(on)}$	-	3.3	5	n secs	$V_{DD}=25V$, $I_D=2A$
Rise time (Notes 1 & 2)		t_r	-	15	25	n secs	
Turn-OFF delay time (Notes 1 & 2)		$t_{d(off)}$	-	17	26	n secs	
Fall time (Notes 1 & 2)		t_f	-	15	25	n secs	

*Measured under pulsed conditions. Width = 300μs. Duty cycle $\leqslant 2\%$.

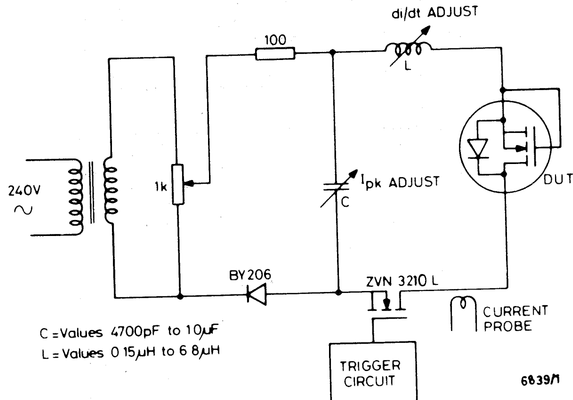
Note 1 Switching times measured with 50 ohm source impedance and <5ns rise time on a pulse generator.

Note 2 Sample test.

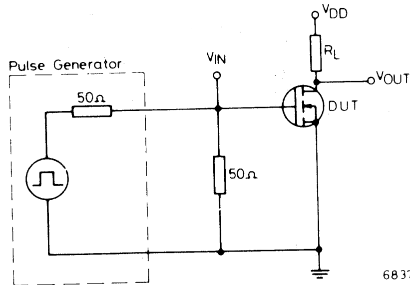
DRAIN-SOURCE DIODE CHARACTERISTICS

Parameter	Symbol	Typ.	Unit	Conditions
Forward ON voltage	V_{SD}	0.86	V	$V_{GS}=0$, $I_S=2.5A$
Reverse recovery time	t_{rr}	108	ns	$V_{GS}=0$, $I_F=2.5A$, $I_R=1.0A$

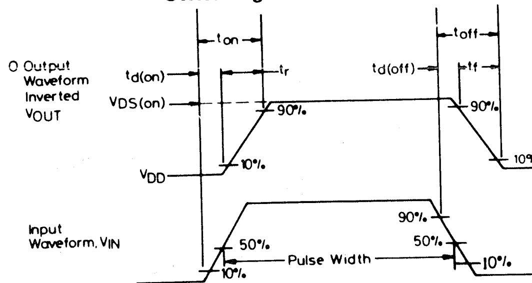
Reverse Recovery Test Circuit



Circuit for Measuring Switching Times



Switching Waveforms



Note
Power MOSFET switching times are essentially independent of operating temperature

ZVN2208B/2210B

Fig. 1 Output Characteristics

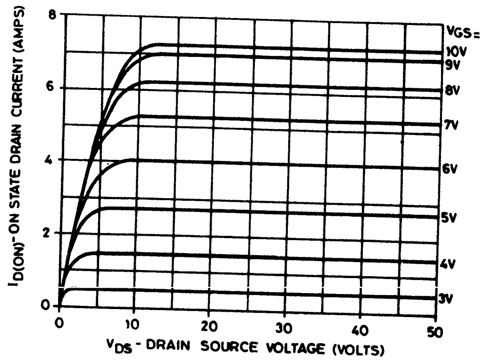


Fig. 2 Saturation Characteristics

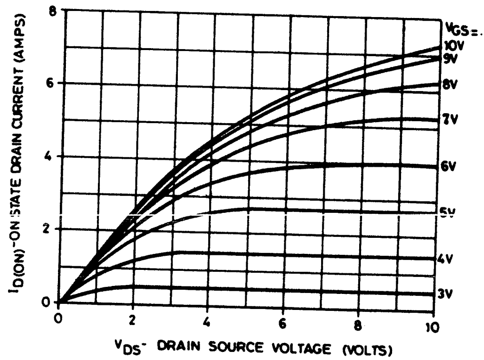


Fig. 3 Voltage Saturation Characteristics

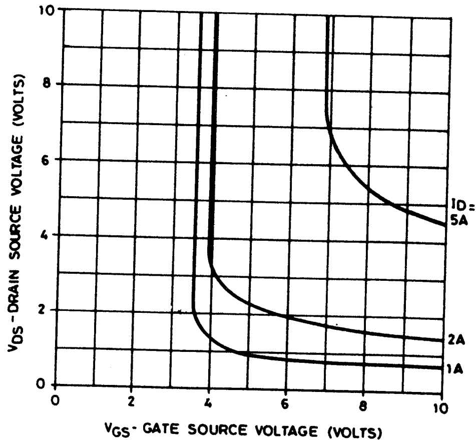


Fig. 4 Transfer Characteristics

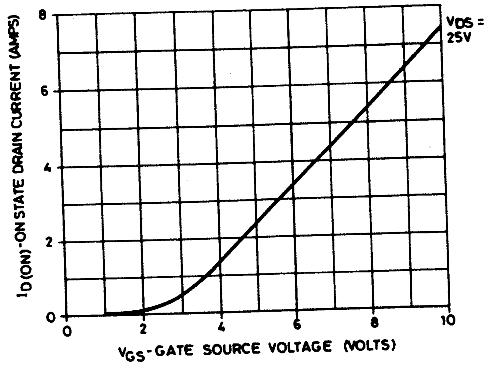


Fig. 5 Capacitance vs Drain-Source Voltage

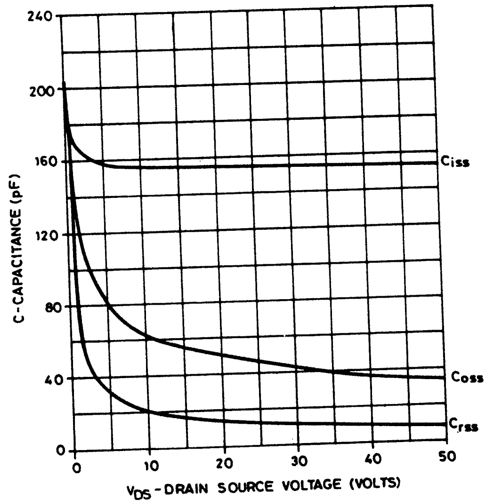


Fig. 6 Transconductance vs Drain-Current

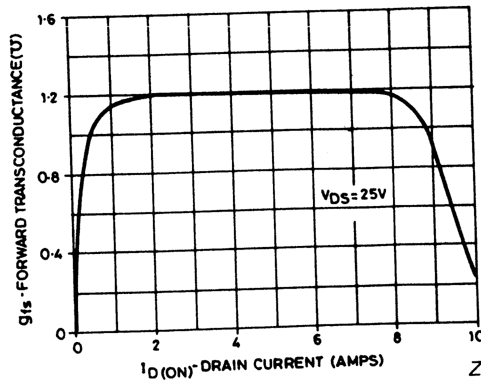


Fig. 7 Transconductance vs Gate-Source Voltage

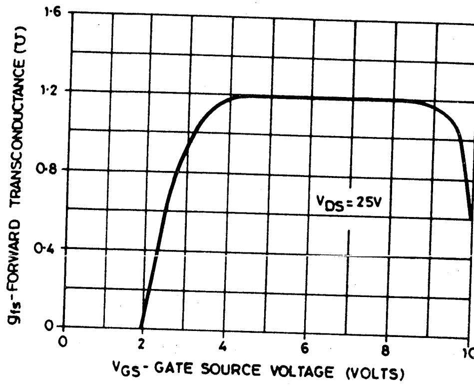


Fig. 8 Gate Charge vs Gate-Source Voltage

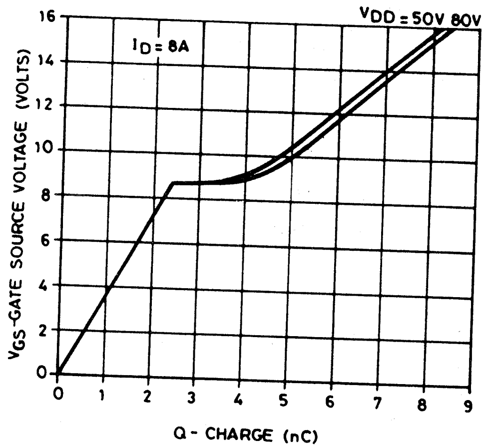


Fig. 9 ON-Resistance vs Gate-Source Voltage

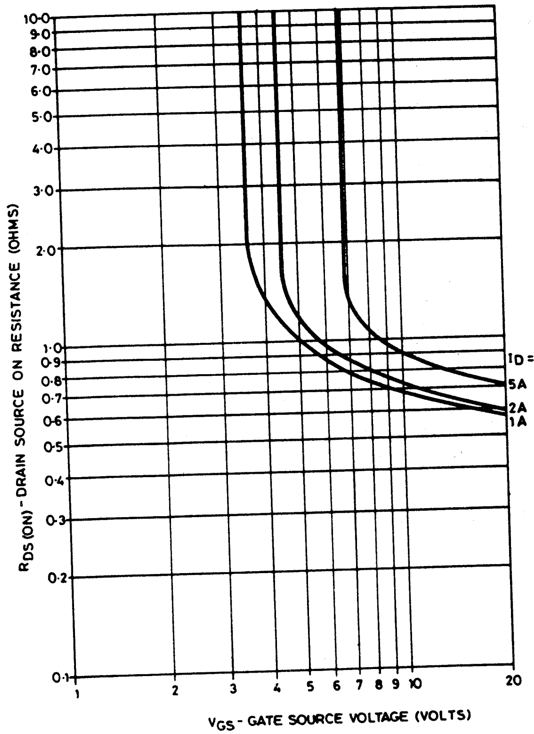
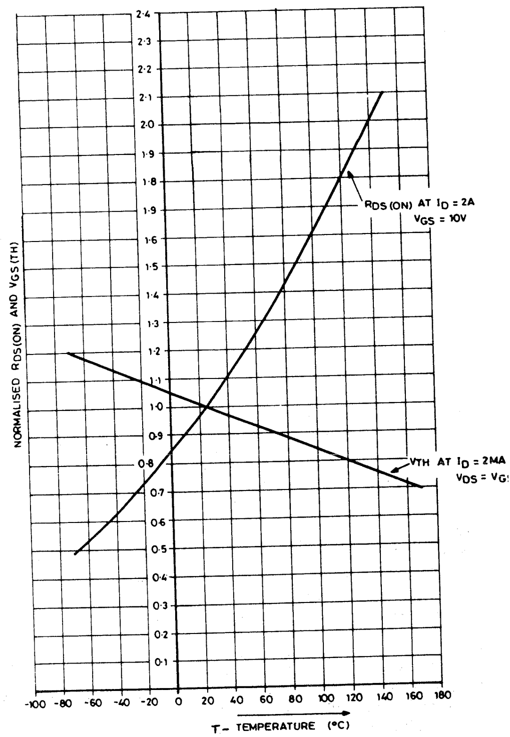


Fig. 10 Variation of $R_{DS(ON)}$ and $V_{GS(th)}$ with Temperature



ZVN2208B/2210B

Fig. 11 Power Derating (Case)

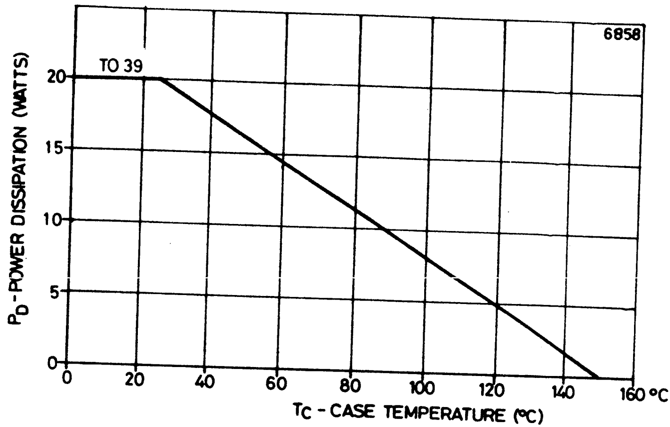
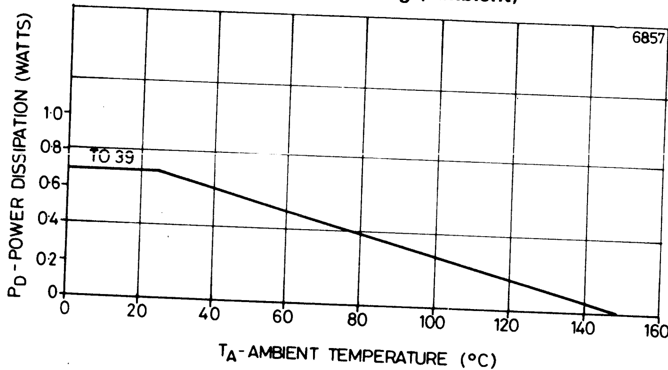


Fig. 12 Power Derating (Ambient)



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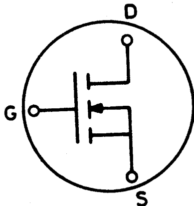
Issue 1, January 1985 5.1M

FERRANTI semiconductors ®

ZVN2208L
ZVN2210L

N-Channel Enhancement-Mode Vertical DMOS Power FET

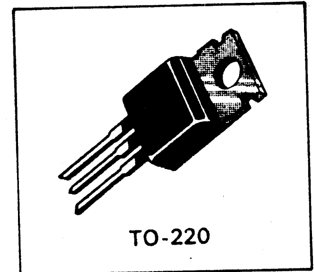
100V: 0.8 ohm: 3.45A



N-Channel

FEATURES

- Compact Geometry
- Fast Switching Speeds
- No Secondary Breakdown
- Excellent Temperature Stability
- High Input Impedance
- Low Current Drive
- Ease of Paralleling



TO-220

DESCRIPTION

Compact OVERLAY (CELL) and INTER-DIGITATED geometries are the basis of the new generation of FERRANTI Power MOSFET transistors. These efficient geometries, optimised for low ON-resistance, low capacitances and fast switching speeds, with computer controlled processing combine to achieve greater device ruggedness.

The planar construction, coupled with ion implantation and the self-aligned poly-silicon gate manufacturing process, provides the reliability and stability in performance required in todays designs.

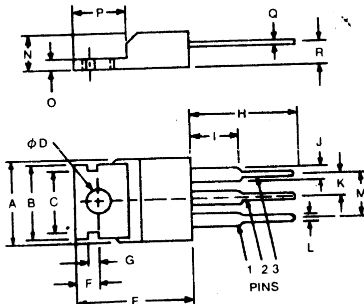
PRODUCT SUMMARY

Device Type	BV_{DSS}	$I_{D(CONT)}$	$R_{D(ON)}$
ZVN2208L	80V	3.45A	0.8Ω
ZVN2210L	100V	3.45A	0.8Ω

Chip Size 0.062″ × 0.072″

FERRANTI Power MOSFETS will directly interface with MICROPROCESSORS, LOGIC ARRAYS and standard IC LOGIC families including CMOS, TTL, PMOS and NMOS.

PACKAGE DIMENSIONS



PIN OUT	
1	Gate
2	Drain & Tab
3	Source

SYMBOL	INCHES		MILLIMETRES	
	MIN	MAX	MIN	MAX
A	.380	.420	9.65	10.66
B	.380	.420	9.65	10.66
C	.300	.320	7.62	8.12
ØD	.139	.147	3.531	3.733
E	.560	.625	14.230	15.870
F	.100	.120	2.54	3.04
G	.040	.060	1.02	1.52
H	.500	.562	12.70	14.27
I		.250		6.35
J	.045	.060	1.14	1.52
K	.090	.110	2.29	2.79
L	.020	.040	.510	1.016
M	.190	.210	4.830	5.330
N	.175	.185	4.445	4.699
O	.030	.055	.762	1.390
P	.230	.270	5.850	6.850
Q	.015	.025	.380	.630
R	.080	.115	2.040	2.920

ZVN2208L/2210L

ABSOLUTE MAXIMUM RATINGS

	Parameters	ZVN2208L	ZVN2210L	Units
V_{DS}	Drain-source voltage	80	100	V
I_D	Continuous drain current (@ $T_A=25°C$)	0.95		A
I_D	Continuous drain current (@ $T_C=25°C$)	3.45		A
I_{DM}	Pulse drain current	12		A
V_{GS}	Gate-source voltage	±20		V
P_D	Max. power dissipation (@ $T_A=25°C$)	1.5		W
P_D	Max. power dissipation (@ $T_C=25°C$)	20		W
	Operating/Storage Temperature Range	−55 to +150		°C

ELECTRICAL CHARACTERISTICS (at T=25°C unless otherwise stated)

Parameter		Symbol	Min.	Typ.	Max.	Unit	Conditions
Drain source breakdown voltage	ZVN2208L	BV_{DSS}	80	-	-	V	$I_D=10\mu A$
	ZVN2210L		100	-	-		$V_{GS}=0$
Gate-source threshold voltage		$V_{GS(th)}$	1	-	3	V	$I_D=2mA$, $V_{DS}=V_{GS}$
Gate body leakage		I_{GSS}	-	1	20	nA	$V_{GS}=\pm20V$, $V_{DS}=0$
Zero gate voltage Drain current (Note 2)		I_{DSS}	-	-	2	μA	V_{DS}=max. rating, $V_{GS}=0$
			-	-	0.2	mA	$V_{DS}=0.8$ × max. rating $V_{GS}=0$ (T=125°C)
On-state drain current*		$I_{D(ON)}$	3	6	-	A	$V_{DS}=25V$, $V_{GS}=10V$
Static drain-source ON-resistance*		$R_{DS(ON)}$	-	-	0.8	Ω	$I_D=2A$, $V_{GS}=10V$
Forward transconductance* (Note 2)		g_{fs}	-	1.2	-	S	$V_{DS}=25V$, $I_D=1.5A$
Input capacitance (Note 2)		C_{iss}	-	160	220	pF	$V_{DS}=25V$
Common source output capacitance (Note 2)		C_{oss}	-	50	75	pF	$V_{GS}=0$
Reverse transfer capacitance (Note 2)		C_{rss}	-	16	25	pF	f=1MHz
Turn-ON delay time (Notes 1 & 2)		$t_{d(on)}$	-	3.3	5	n secs	$V_{DD}=25V$
Rise time (Notes 1 & 2)		t_r	-	15	25	n secs	
Turn-OFF delay time (Notes 1 & 2)		$t_{d(off)}$	-	17	26	n secs	$I_D=2A$
Fall time (Notes 1 & 2)		t_f	-	15	25	n secs	

*Measured under pulsed conditions. Width=300μs. Duty cycle ≤2%.

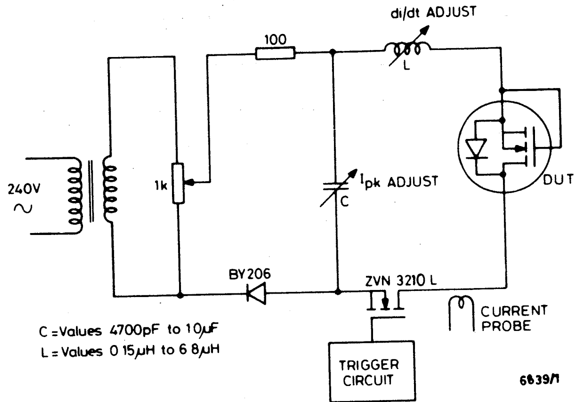
Note 1 Switching times measured with 50 ohm source impedance and <5ns rise time on a pulse generator.

Note 2 Sample test.

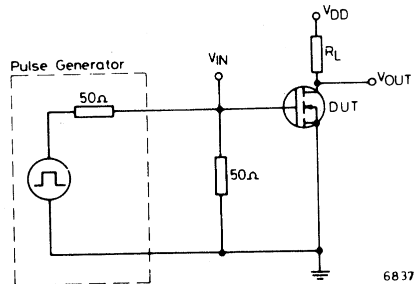
DRAIN-SOURCE DIODE CHARACTERISTICS

Parameter	Symbol	Typ.	Unit	Conditions
Forward ON voltage	V_{SD}	0.89	V	$V_{GS}=0$, $I_S=3A$
Reverse recovery time	t_{rr}	124	ns	$V_{GS}=0$, $I_F=3A$, $I_R=1A$

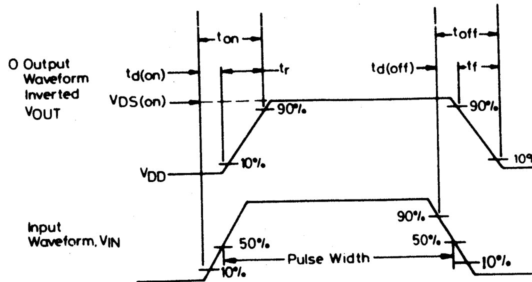
Reverse Recovery Test Circuit



Circuit for Measuring Switching Times



Switching Waveforms



Note
Power MOSFET switching times are essentially independent of operating temperature

ZVN2208L/2210L

Fig. 1 Output Characteristics

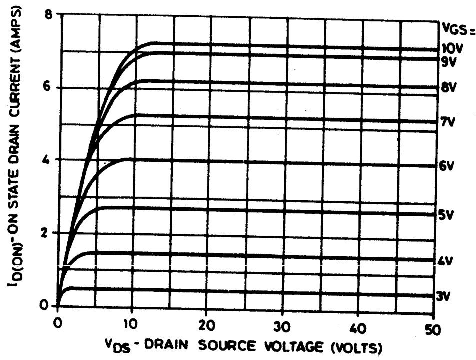


Fig. 2 Saturation Characteristics

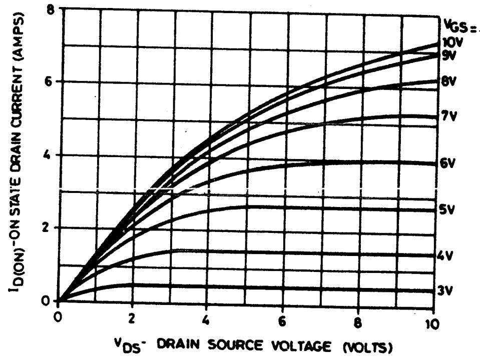


Fig. 3 Voltage Saturation Characteristics

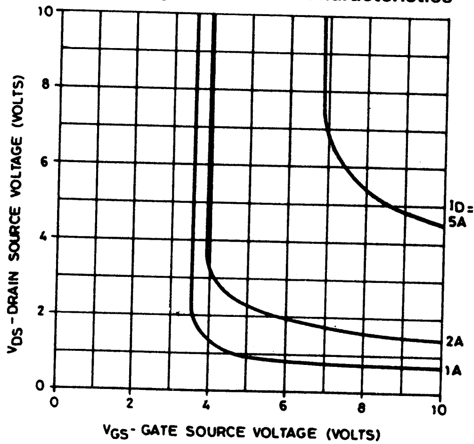


Fig. 4 Transfer Characteristics

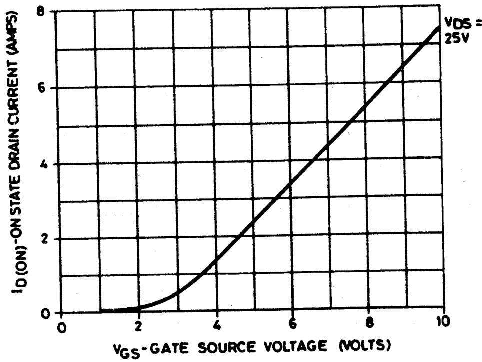


Fig. 5 Capacitance vs Drain-Source Voltage

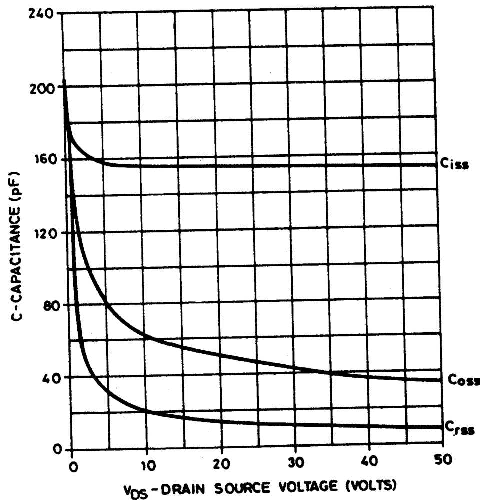


Fig. 6 Transconductance vs Drain-Current

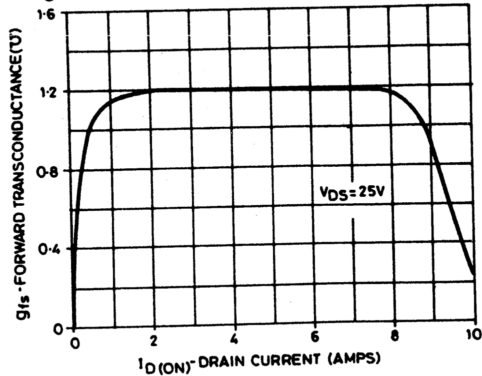


Fig. 7 Transconductance vs Gate-Source Voltage

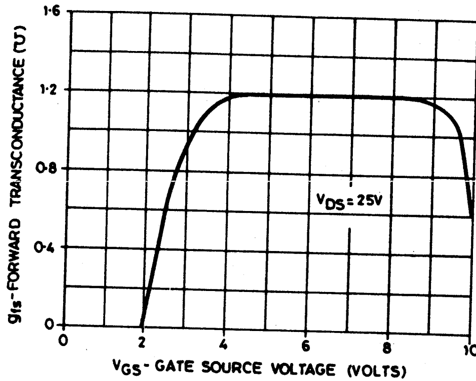


Fig. 8 Gate Charge vs Gate-Source Voltage

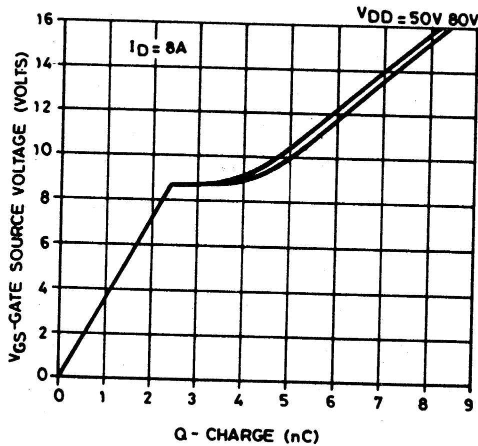


Fig. 9 ON-Resistance vs Gate-Source Voltage

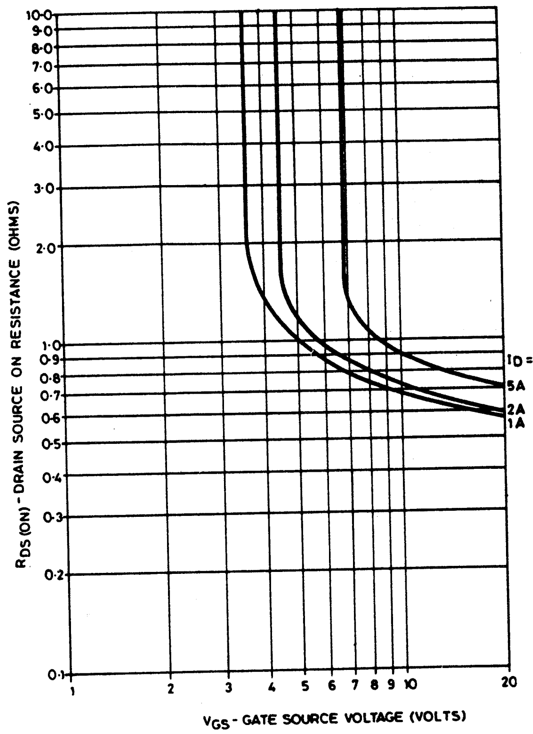


Fig. 10 Variation of $R_{DS(ON)}$ and $V_{GS(th)}$ with Temperature

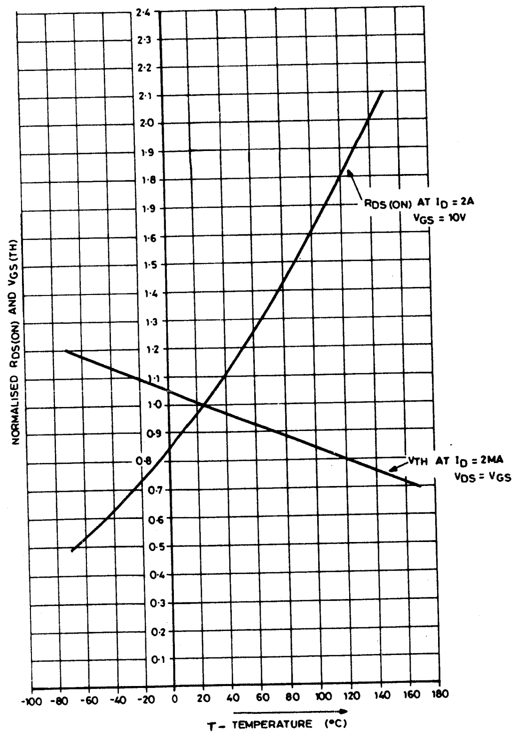


Fig. 11 Power Derating (Case)

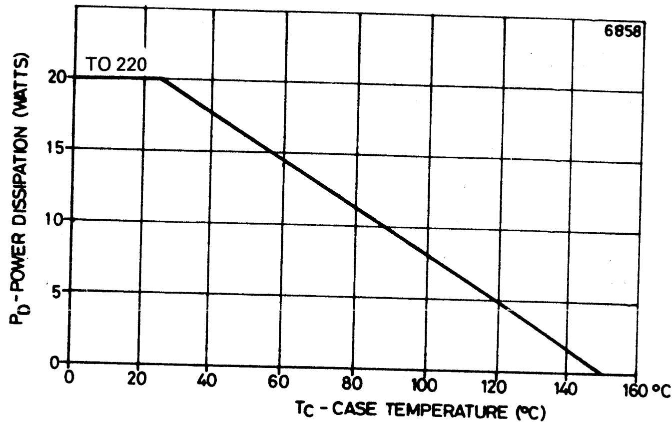
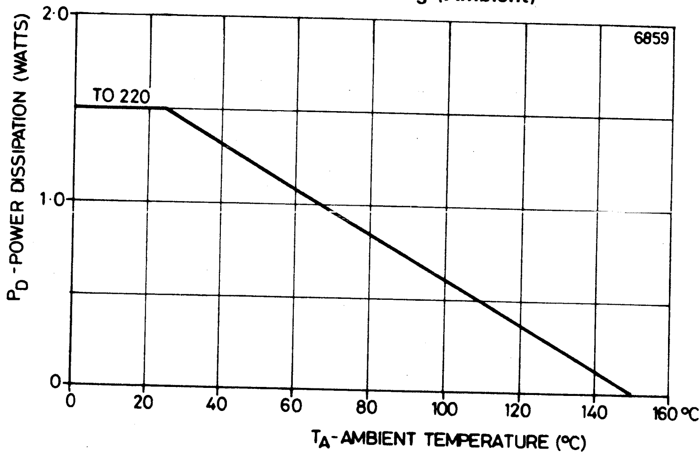


Fig. 12 Power Derating (Ambient)



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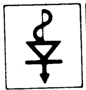
Issue 1, January 1985 5.1M

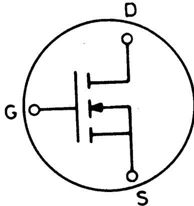


FERRANTI
semiconductors ®

ZVN2215B
ZVN2220B

N-Channel Enhancement-Mode Vertical DMOS Power FET

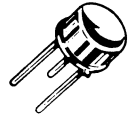
200V: 2.5 ohm: 1.85A



N-Channel

FEATURES

- Compact Geometry
- Fast Switching Speeds
- No Secondary Breakdown
- Excellent Temperature Stability
- High Input Impedance
- Low Current Drive
- Ease of Paralleling



TO-39 PACKAGE

DESCRIPTION

Compact OVERLAY (CELL) and INTER-DIGITATED geometries are the basis of the new generation of FERRANTI Power MOSFET transistors. These efficient geometries, optimised for low ON-resistance, low capacitances and fast switching speeds, with computer controlled processing combine to achieve greater device ruggedness.

The planar construction, coupled with ion implantation and the self-aligned poly-silicon gate manufacturing process, provides the reliability and stability in performance required in todays designs.

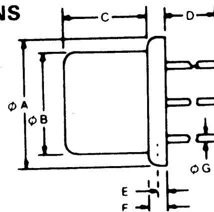
PRODUCT SUMMARY

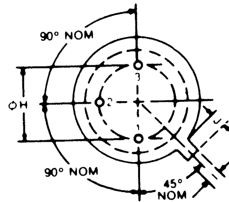
Device Type	BV_{DSS}	$I_{D(CONT)}$	$R_{D(ON)}$
ZVN2215B	150V	1.85A	2.5Ω
ZVN2220B	200V	1.85A	2.5Ω

Chip Size 0.062″ × 0.072″

FERRANTI Power MOSFETS will directly interface with MICROPROCESSORS, LOGIC ARRAYS and standard IC LOGIC families including CMOS, TTL, PMOS and NMOS.

PACKAGE DIMENSIONS





SYMBOL	INCHES		MILLIMETRES	
	MIN	MAX	MIN	MAX
ØA	.350	.370	8.89	9.40
ØB	.306	.335	7.77	8.51
C	.240	.260	6.10	6.60
D	.500		12.70	
E	.009	.023	.229	.584
F	.018	.045	.458	1.143
ØG	.016	.021	.406	.533
ØH	.190	.210	4.83	5.33
I	.028	.037	.711	.939
J	.026	.040	.660	1.016

PIN OUT	
1	Source
2	Gate
3	Drain & Case

ZVN2215B/2220B

ABSOLUTE MAXIMUM RATINGS

	Parameters	ZVN2215B	ZVN2220B	Units
V_{DS}	Drain-source voltage	150	200	V
I_D	Continuous drain current (@ $T_A = 25°C$)	0.35		A
I_D	Continuous drain current (@ $T_C = 25°C$)	1.85		A
I_{DM}	Pulse drain current	8		A
V_{GS}	Gate-source voltage	± 20		V
P_D	Max. power dissipation (@ $T_A = 25°C$)	0.7		W
P_D	Max. power dissipation (@ $T_C = 25°C$)	20		W
	Operating/Storage Temperature Range	−55 to +150		°C

ELECTRICAL CHARACTERISTICS (at T = 25°C unless otherwise stated)

Parameter		Symbol	Min.	Typ.	Max.	Unit	Conditions
Drain source breakdown voltage	ZVN2215B	BV_{DSS}	150	-	-	V	$I_D = 10\mu A$, $V_{GS} = 0$
	ZVN2220B		200	-	-		
Gate-source threshold voltage		$V_{GS(th)}$	1	-	3	V	$I_D = 2mA$, $V_{DS} = V_{GS}$
Gate body leakage		I_{GSS}	-	1	20	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0$
Zero gate voltage Drain current		I_{DSS}	-	-	10	μA	V_{DS} = max. rating, $V_{GS} = 0$
(Note 2)			-	-	0.2	mA	$V_{DS} = 0.8 \times$ max. rating $V_{GS} = 0$ (T = 125°C)
On-state drain current*		$I_{D(ON)}$	2	3	-	A	$V_{DS} = 25V$, $V_{GS} = 10V$
Static drain-source ON-resistance*		$R_{DS(ON)}$	-	-	2.5	Ω	$I_D = 1A$, $V_{GS} = 10V$
Forward transconductance* (Note 2)		g_{fs}	-	1.0	-	S	$V_{DS} = 25V$, $I_D = 1A$
Input capacitance (Note 2)		C_{iss}	-	170	200	pF	$V_{DS} = 25V$, $V_{GS} = 0$, f = 1MHz
Common source output capacitance (Note 2)		C_{oss}	-	30	45	pF	
Reverse transfer capacitance (Note 2)		C_{rss}	-	6	10	pF	
Turn-ON delay time (Notes 1 & 2)		$t_{d(on)}$	-	3	6	n secs	$V_{DD} = 25V$, $I_D = 1A$
Rise time (Notes 1 & 2)		t_r	-	6	10	n secs	
Turn-OFF delay time (Notes 1 & 2)		$t_{d(off)}$	-	20	26	n secs	
Fall time (Notes 1 & 2)		t_f	-	11	15	n secs	

*Measured under pulsed conditions. Width = 300μs. Duty cycle $\leqslant$ 2%.

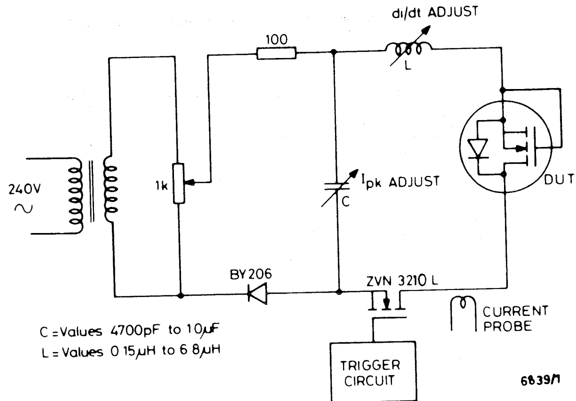
Note 1 Switching times measured with 50 ohm source impedance and <5ns rise time on a pulse generator.

Note 2 Sample test.

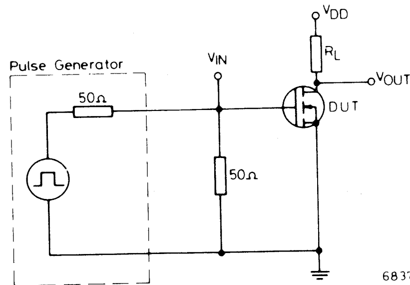
DRAIN-SOURCE DIODE CHARACTERISTICS

Parameter	Symbol	Typ.	Unit	Conditions
Forward ON voltage	V_{SD}	0.83	V	$V_{GS}=0$, $I_S=1.7A$
Reverse recovery time	t_{rr}	150	ns	$V_{GS}=0$, $I_F=1.7A$, $I_R=1.0A$

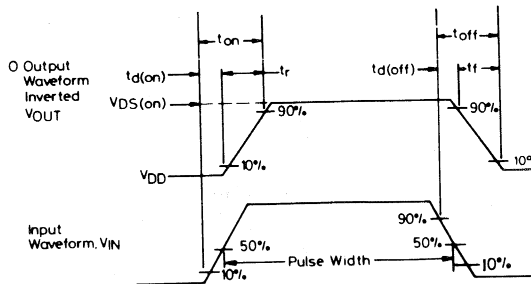
Reverse Recovery Test Circuit



Circuit for Measuring Switching Times



Switching Waveforms



Note
Power MOSFET switching times are essentially independent of operating temperature

Fig. 1 Output Characteristics

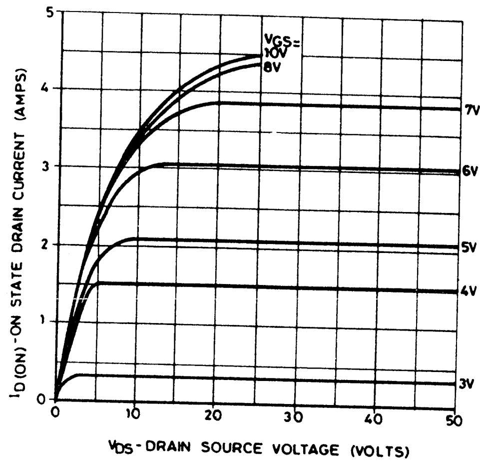


Fig. 2 Saturation Characteristics

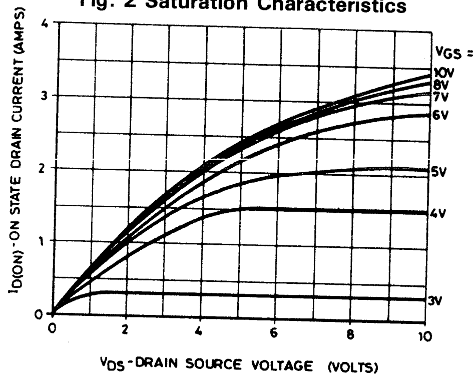


Fig. 3 Voltage Saturation Characteristics

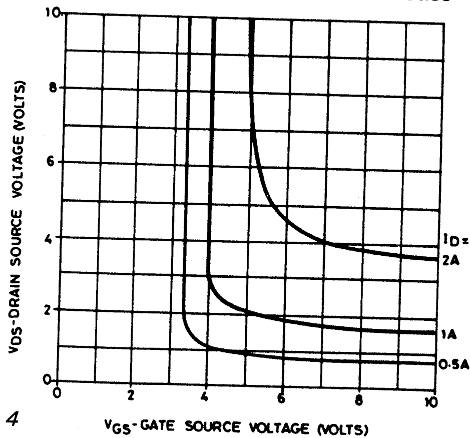


Fig. 4 Transfer Characteristics

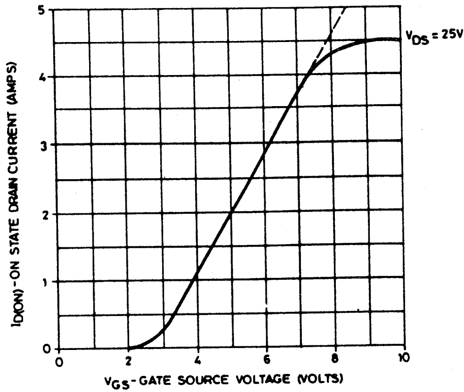


Fig. 5 Capacitance vs Drain-Source Voltage

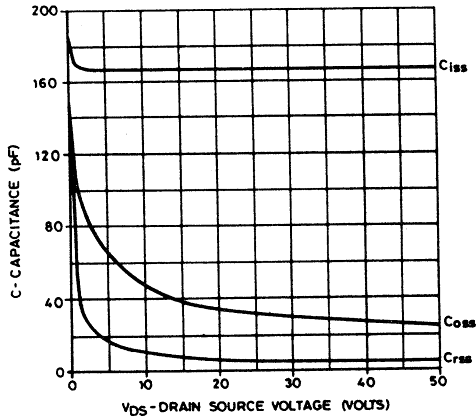


Fig. 6 Transconductance vs Drain-Current

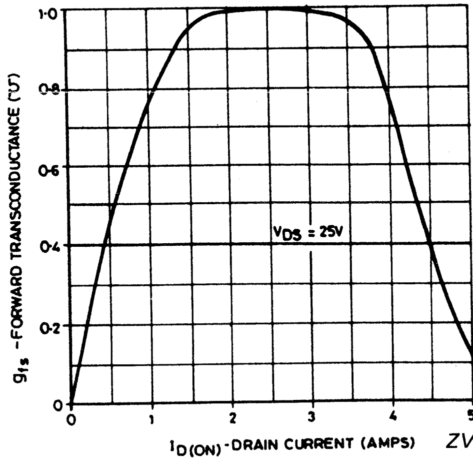


Fig. 7 Transconductance vs Gate-Source Voltage

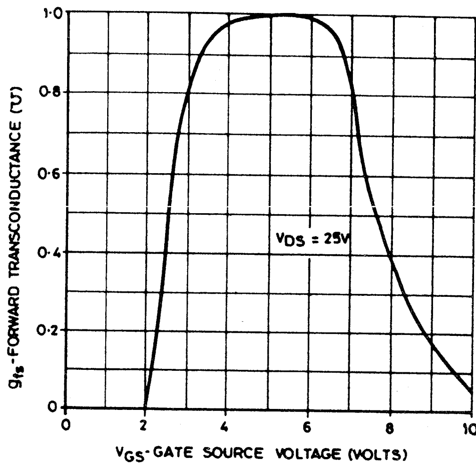


Fig. 8 Gate Charge vs Gate-Source Voltage

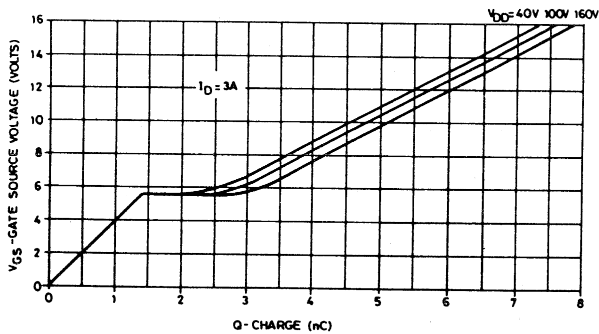


Fig. 9 ON-Resistance vs Gate-Source Voltage

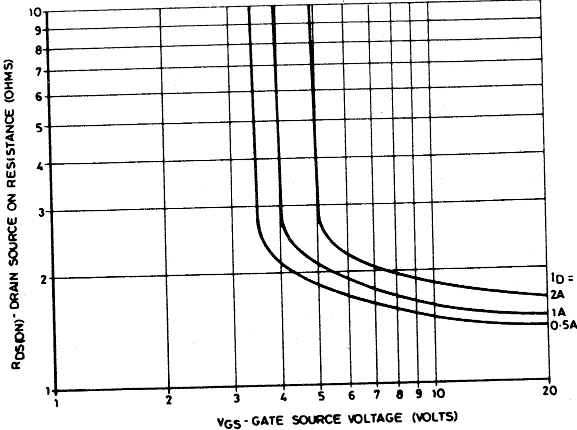


Fig. 10 Variation of $R_{DS(ON)}$ and $V_{GS(th)}$ with Temperature

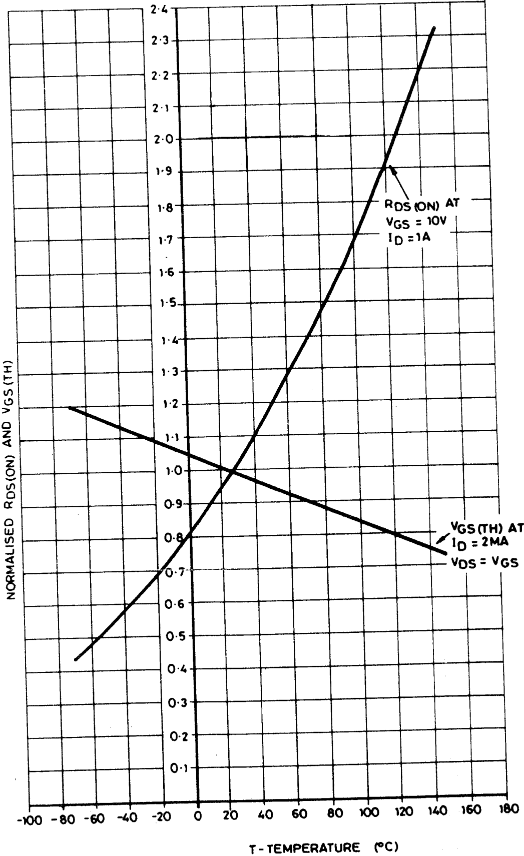


Fig. 11 Power Derating (Case)

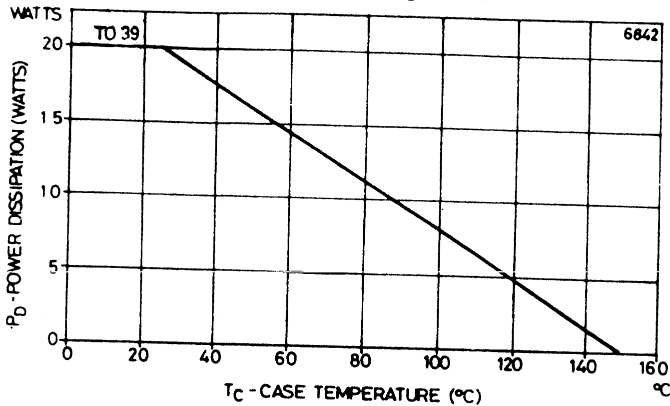
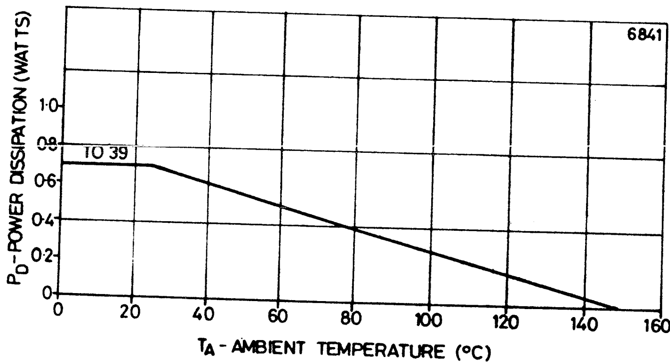


Fig. 12 Power Derating (Ambient)



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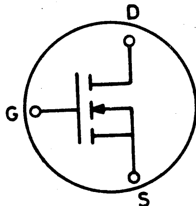
Issue 1, January 1985 5.1M

FERRANTI semiconductors ®

ZVN2215L
ZVN2220L

N-Channel Enhancement-Mode Vertical DMOS Power FET

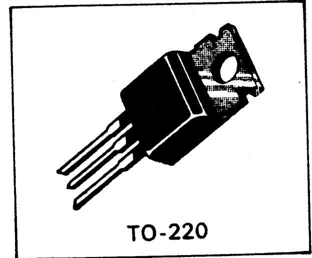
200V: 2.5 ohm: 1.85A



N-Channel

FEATURES

- Compact Geometry
- Fast Switching Speeds
- No Secondary Breakdown
- Excellent Temperature Stability
- High Input Impedance
- Low Current Drive
- Ease of Paralleling


TO-220

DESCRIPTION

Compact OVERLAY (CELL) and INTER-DIGITATED geometries are the basis of the new generation of FERRANTI Power MOSFET transistors. These efficient geometries, optimised for low ON-resistance, low capacitances and fast switching speeds, with computer controlled processing combine to achieve greater device ruggedness.

The planar construction, coupled with ion implantation and the self-aligned poly-silicon gate manufacturing process, provides the reliability and stability in performance required in todays designs.

PRODUCT SUMMARY

Device Type	BV_{DSS}	$I_{D(CONT)}$	$R_{D(ON)}$
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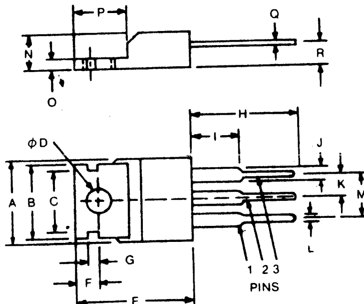
ZVN2220L	200V	1.85A	2.5Ω

Chip Size 0.062″ × 0.072″

FERRANTI Power MOSFETS will directly interface with MICROPROCESSORS, LOGIC ARRAYS and standard IC LOGIC families including CMOS, TTL, PMOS and NMOS.

PACKAGE DIMENSIONS



PIN OUT	
1	Gate
2	Drain & Tab
3	Source

SYMBOL	INCHES		MILLIMETRES	
	MIN	MAX	MIN	MAX
A	.380	.420	9.65	10.66
B	.380	.420	9.65	10.66
C	.300	.320	7.62	8.12
ØD	.139	.147	3.531	3.733
E	.560	.625	14.230	15.870
F	.100	.120	2.54	3.04
G	.040	.060	1.02	1.52
H	.500	.562	12.70	14.27
I		.250		6.35
J	.045	.060	1.14	1.52
K	.090	.110	2.29	2.79
L	.020	.040	.510	1.016
M	.190	.210	4.830	5.330
N	.175	.185	4.445	4.699
O	.030	.055	.762	1.390
P	.230	.270	5.850	6.850
Q	.015	.025	.380	.630
R	.080	.115	2.040	2.920

ZVN2215L/2220L

ABSOLUTE MAXIMUM RATINGS

Parameters		ZVN2215L	ZVN2220L	Units
V_{DS}	Drain-source voltage	150	200	V
I_D	Continuous drain current (@ $T_A=25°C$)	0.5		A
I_D	Continuous drain current (@ $T_C=25°C$)	1.85		A
I_{DM}	Pulse drain current	8		A
V_{GS}	Gate-source voltage	±20		V
P_D	Max. power dissipation (@ $T_A=25°C$)	1.5		W
P_D	Max. power dissipation (@ $T_C=25°C$)	20		W
	Operating/Storage Temperature Range	−55 to +150		°C

ELECTRICAL CHARACTERISTICS (at T=25°C unless otherwise stated)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Drain source breakdown voltage ZVN2215L	BV_{DSS}	150	-	-	V	$I_D=10\mu A$
Drain source breakdown voltage ZVN2220L	BV_{DSS}	200	-	-	V	$V_{GS}=0$
Gate-source threshold voltage	$V_{GS(th)}$	1	-	3	V	$I_D=2mA$, $V_{DS}=V_{GS}$
Gate body leakage	I_{GSS}	-	1	20	nA	$V_{GS}=\pm 20V$, $V_{DS}=0$
Zero gate voltage Drain current (Note 2)	I_{DSS}	-	-	10	μA	V_{DS}=max. rating, $V_{GS}=0$
		-	-	0.2	mA	$V_{DS}=0.8\times$ max. rating $V_{GS}=0$ (T=125°C)
On-state drain current*	$I_{D(ON)}$	2	3	-	A	$V_{DS}=25V$, $V_{GS}=10V$
Static drain-source ON-resistance*	$R_{DS(ON)}$	-	-	2.5	Ω	$I_D=1A$, $V_{GS}=10V$
Forward transconductance* (Note 2)	g_{fs}	-	1.0	-	S	$V_{DS}=25V$, $I_D=1A$
Input capacitance (Note 2)	C_{iss}	-	170	220	pF	$V_{DS}=25V$
Common source output capacitance (Note 2)	C_{oss}	-	30	45	pF	$V_{GS}=0$
Reverse transfer capacitance (Note 2)	C_{rss}	-	6	10	pF	f=1MHz
Turn-ON delay time (Notes 1 & 2)	$t_{d(on)}$	-	3	6	n secs	$V_{DD}=25V$
Rise time (Notes 1 & 2)	t_r	-	6	10	n secs	
Turn-OFF delay time (Notes 1 & 2)	$t_{d(off)}$	-	20	26	n secs	$I_D=1A$
Fall time (Notes 1 & 2)	T_f	-	11	15	n secs	

*Measured under pulsed conditions. Width=300μs. Duty cycle ⩽2%.

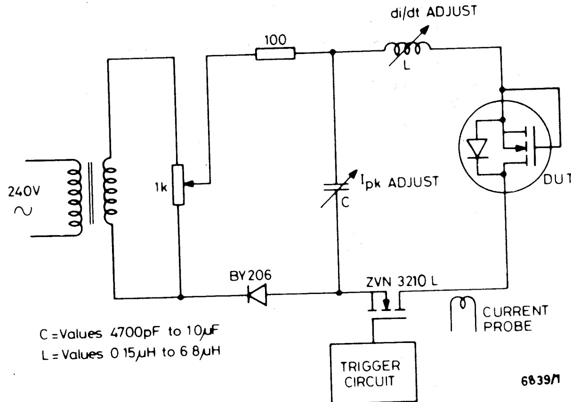
Note 1 Switching times measured with 50 ohm source impedance and <5ns rise time on a pulse generator.

Note 2 Sample test.

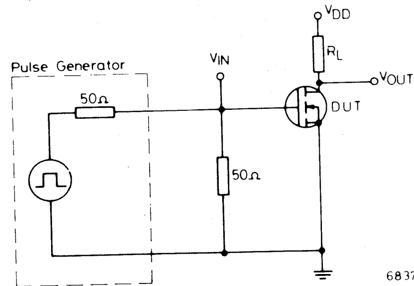
DRAIN-SOURCE DIODE CHARACTERISTICS

Parameter	Symbol	Typ.	Unit	Conditions
Forward ON voltage	V_{SD}	0.85	V	$V_{GS}=0,\ I_S=2A$
Reverse recovery time	t_{rr}	175	ns	$V_{GS}=0,\ I_F=2A,\ I_R=1A$

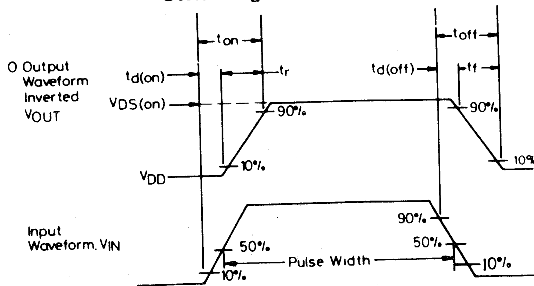
Reverse Recovery Test Circuit



Circuit for Measuring Switching Times



Switching Waveforms



Note
Power MOSFET switching times are essentially independent of operating temperature

ZVN2215L/2220L

Fig. 1 Output Characteristics

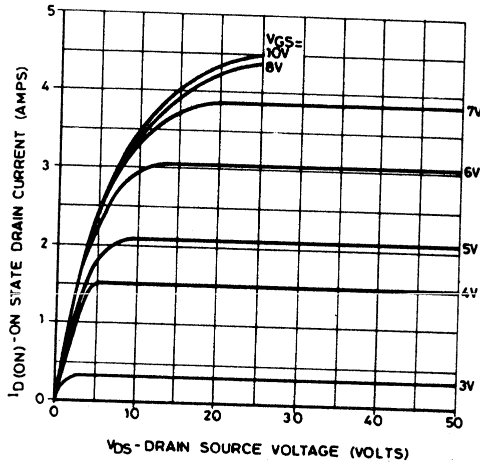


Fig. 2 Saturation Characteristics

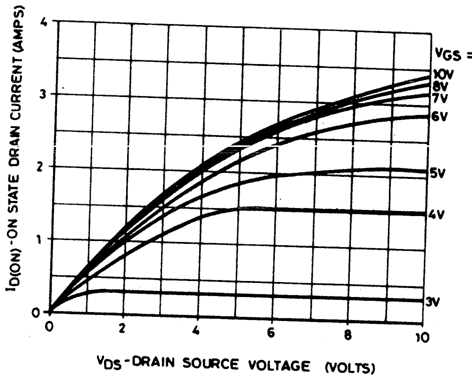


Fig. 3 Voltage Saturation Characteristics

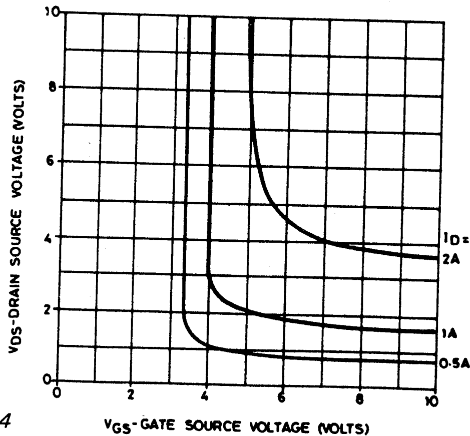


Fig. 4 Transfer Characteristics

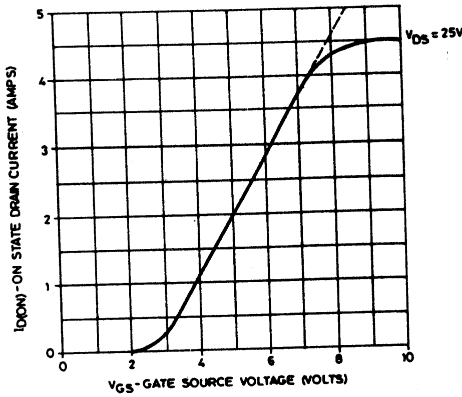


Fig. 5 Capacitance vs Drain-Source Voltage

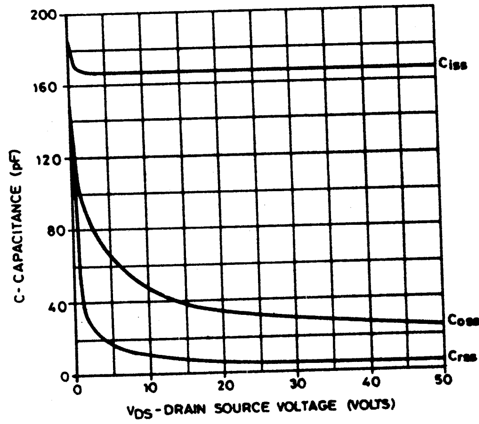


Fig. 6 Transconductance vs Drain-Current

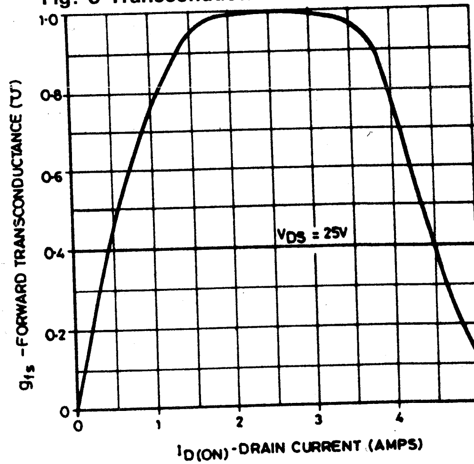


Fig. 7 Transconductance vs Gate-Source Voltage

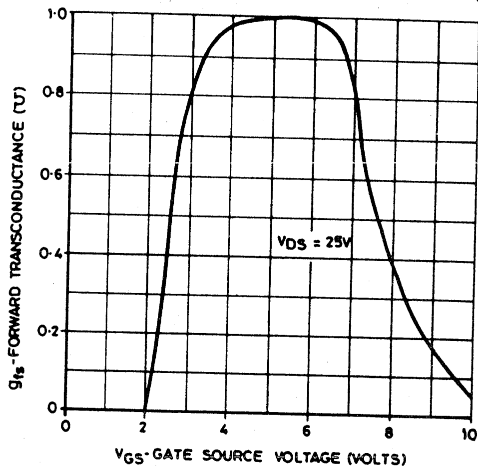


Fig. 8 Gate Charge vs Gate-Source Voltage

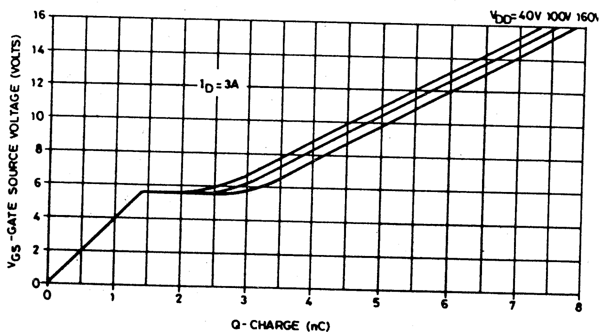


Fig. 9 ON-Resistance vs Gate-Source Voltage

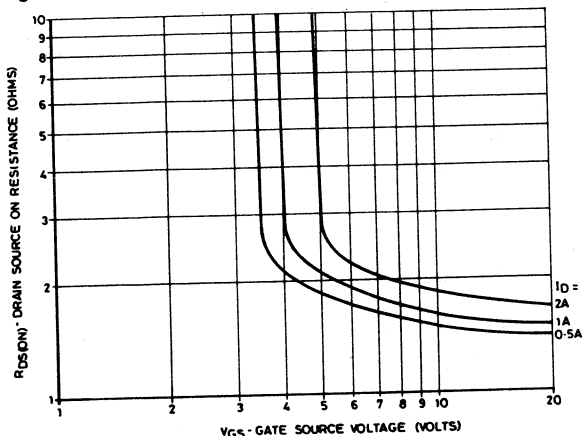
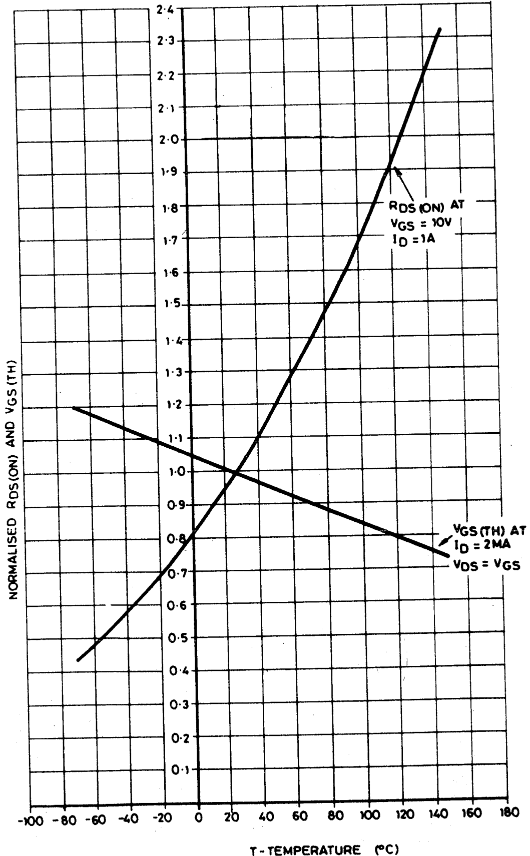


Fig. 10 Variation of $R_{DS(ON)}$ and $V_{GS(th)}$ with Temperature



ZVN2215L/2220L

Fig. 11 Power Derating (Case)

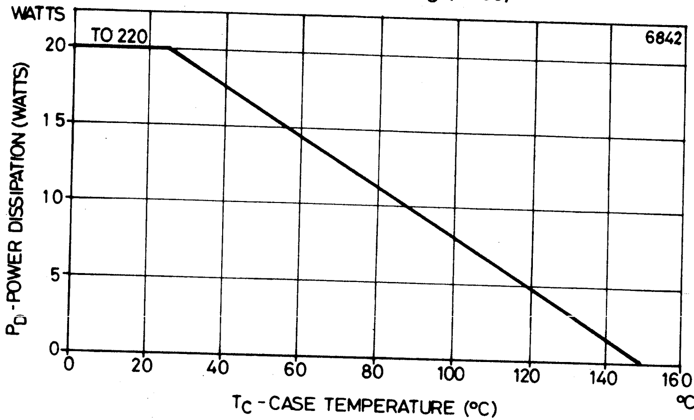
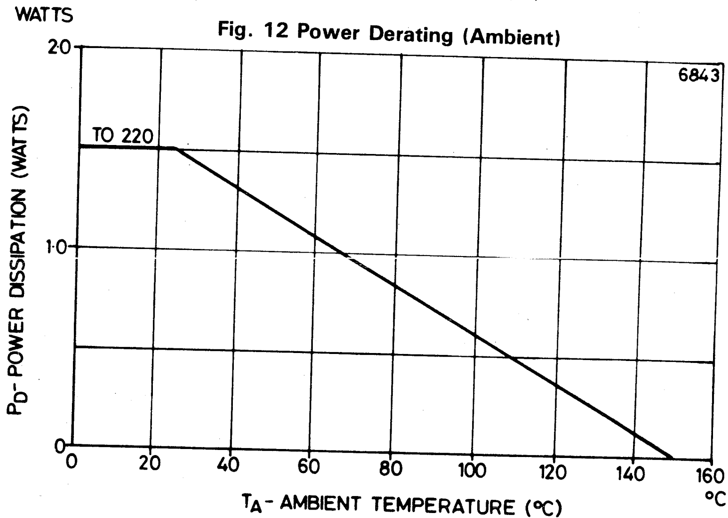


Fig. 12 Power Derating (Ambient)



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Issue 1, January 1985 5.1M

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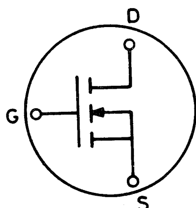
ZVN2224B/L

N-Channel Enhancement-Mode Vertical DMOS Power FET

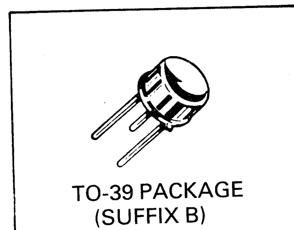
240V: 6 ohm:



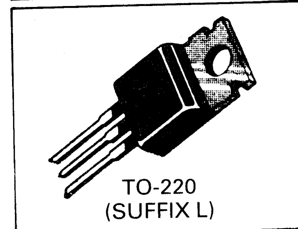
N-Channel

FEATURES

- Compact Geometry
- Fast Switching Speeds
- No Secondary Breakdown
- Excellent Temperature Stability
- High Input Impedance
- Low Current Drive
- Ease of Paralleling



TO-39 PACKAGE (SUFFIX B)



TO-220 (SUFFIX L)

DESCRIPTION

Compact OVERLAY (CELL) and INTER-DIGITATED geometries are the basis of the new generation of FERRANTI Power MOSFET transistors. These efficient geometries, optimised for low ON-resistance, low capacitances and fast switching speeds, with computer controlled processing combine to achieve greater device ruggedness.

The planar construction, coupled with ion implantation and the self-aligned poly-silicon gate manufacturing process, provides the reliability and stability in performance required in todays designs.

FERRANTI Power MOSFETS will directly interface with MICROPROCESSORS, LOGIC ARRAYS and standard IC LOGIC families including CMOS, TTL, PMOS and NMOS.

PRODUCT SUMMARY

TO-39

Device Type	BV_{DSS}	$I_{D(CONT)}$	$R_{D(ON)}$
ZVN2224B	240V	1.2A	6Ω

TO-220

Device Type	BV_{DSS}	$I_{D(CONT)}$	$R_{D(ON)}$
ZVN2224L	240V	1.2A	6Ω

Chip Size 0.062″ × 0.072″

ZVN2224B/L

ABSOLUTE MAXIMUM RATINGS

Parameters		ZVN2224		Units
V_{DS}	Drain-source voltage	240		V
I_D	Continuous drain current (@ $T_A = 25°C$)	0.23 (TO-39)	0.33 (TO-220)	A
I_D	Continuous drain current (@ $T_C = 25°C$)	1.2		A
I_{DM}	Pulse drain current	6		A
V_{GS}	Gate-source voltage	±20		V
P_D	Max. power dissipation (@ $T_A = 25°C$)	0.7 (TO-39)	1.5 (TO-220)	W
P_D	Max. power dissipation (@ $T_C = 25°C$)	20		W
	Operating/Storage Temperature Range	−55 to +150		°C

ELECTRICAL CHARACTERISTICS (at T = 25°C unless otherwise stated)

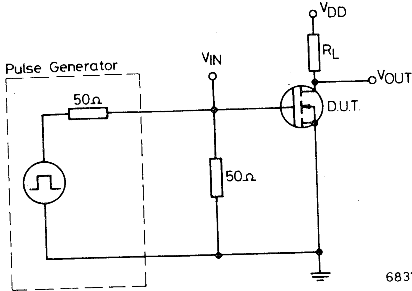
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Drain source breakdown voltage	BV_{DSS}	240	-	-	V	$I_D = 10\mu A$, $V_{GS} = 0$
Gate-source threshold voltage	$V_{GS(th)}$	1	-	3	V	$I_D = 2mA$, $V_{DS} = V_{GS}$
Gate body leakage	I_{GSS}	-	-	20	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0$
Zero gate voltage Drain current (Note 2)	I_{DSS}	-	-	10	μA	V_{DS} = max. rating, $V_{GS} = 0$
		-	-	0.2	mA	$V_{DS} = 0.8 \times$ max. rating $V_{GS} = 0$ ($T = 125°C$)
On-state drain current*	$I_{D(ON)}$	1.5	2	-	A	$V_{DS} = 25V$, $V_{GS} = 10V$
Static drain-source ON-resistance*	$R_{DS(ON)}$	-	4	6	Ω	$I_D = 1A$, $V_{GS} = 10V$
Forward transconductance* (Note 2)	g_{fs}	-	750	-	mS	$V_{DS} = 25V$, $I_D = 1A$
Input capacitance (Note 2)	C_{iss}	-	-	220	pF	$V_{DS} = 25V$
Common source output capacitance (Note 2)	C_{oss}	-	-	45		$V_{GS} = 0$
Reverse transfer capacitance (Note 2)	C_{rss}	-	-	10		$f = 1MHz$
Turn-ON delay time (Notes 1 & 2)	$t_{d(on)}$	-	-	6	n secs	$V_{DD} = 25V$
Rise time (Notes 1 & 2)	t_r	-	-	10		
Turn-OFF delay time (Notes 1 & 2)	$t_{d(off)}$	-	-	26		$I_D = 1A$
Fall time (Notes 1 & 2)	t_f	-	-	15		

*Measured under pulsed conditions. Width = 300μs. Duty cycle ⩽ 2%.

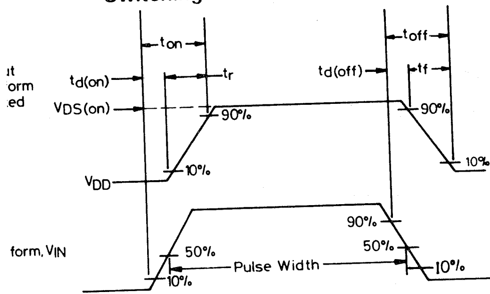
Note 1 Switching times measured with 50 ohm source impedance and <5ns rise time on a pulse generator.

Note 2 Sample test.

Circuit for Measuring Switching Times



Switching Waveforms

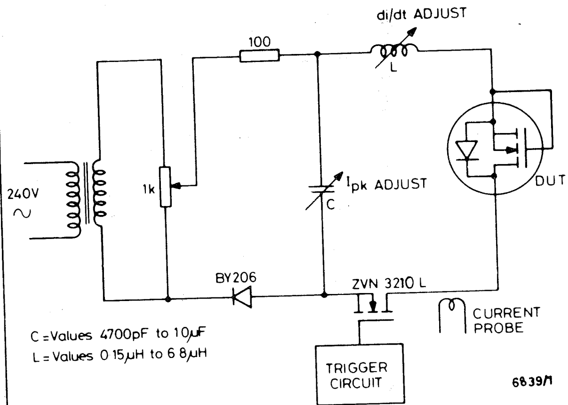


Input voltage amplitude 10 Volts peak

6838/1

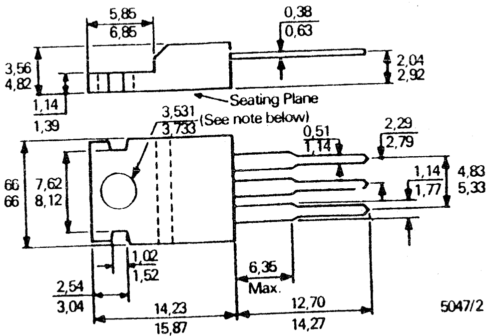
r MOSFET switching
; are essentially independent
erating temperature

Reverse Recovery Test Circuit



PACKAGE OUTLINE

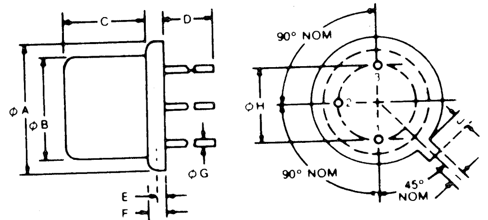
TO-220 (All dimensions are in millimetres)



Note: The tab is connected to the

JEDEC: TO-220AB

TO-39



PIN OUT	
1	Source
2	Gate
3	Drain & Case

SYMBOL	INCHES		MILLIMETRES	
	MIN	MAX	MIN	MAX
ØA	.350	.370	8.89	9.40
ØB	.306	.335	7.77	8.51
C	.240	.260	6.10	6.60
D	.500		12.70	
E	.009	.023	.229	.584
F	.018	.045	.458	1.143
ØG	.016	.021	.406	.533
ØH	.190	.210	4.83	5.33
I	.028	.037	.711	.939
J	.026	.040	.660	1.016

Fig. 11 Power Derating (Case)

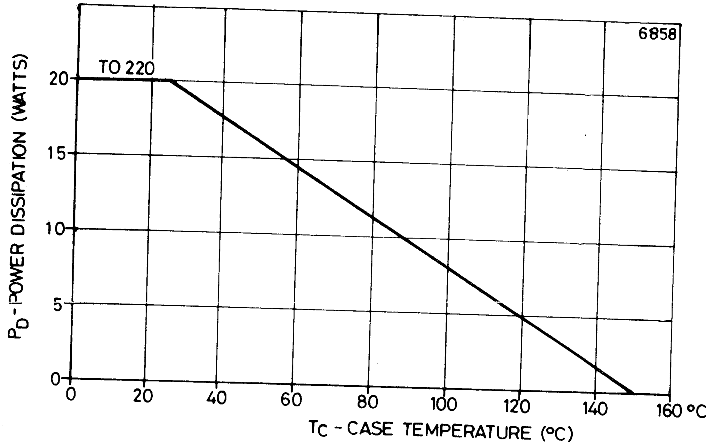
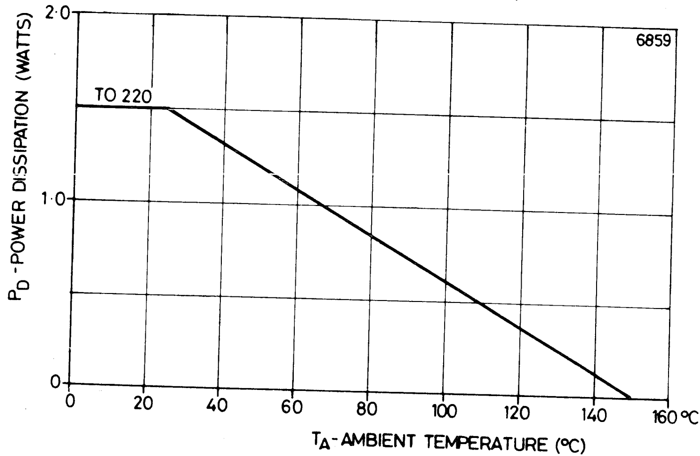


Fig. 12 Power Derating (Ambient)



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Issue 1, January 1985 5.1M

Section 4

ZVN05 Range

ZVN0526A

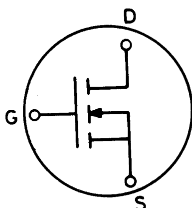
ZVN0535A/B/L

FERRANTI semiconductors ®

ZVN0526A

N-Channel Enhancement-Mode Vertical DMOS Power FET

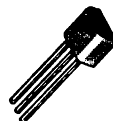
260V: 40 ohm: 100mA



N-Channel

FEATURES

- Compact Geometry
- Fast Switching Speeds
- No Secondary Breakdown
- Excellent Temperature Stability
- High Input Impedance
- Low Current Drive



PLASTIC E-LINE (TO-92)

DESCRIPTION

Compact OVERLAY (CELL) and INTER-DIGITATED geometries are the basis of the new generation of FERRANTI Power MOSFET transistors. These efficient geometries, optimised for low ON-resistance, low capacitances and fast switching speeds, with computer controlled processing combine to achieve greater device ruggedness.

The planar construction, coupled with ion implantation and the self-aligned poly-silicon gate manufacturing process, provides the reliability and stability in performance required in todays designs.

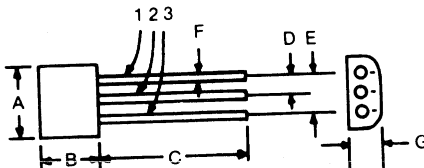
PRODUCT SUMMARY

Device Type	BV_{DSS}	$I_{D(CONT)}$	$R_{D(ON)}$
ZVN0526A	260V	0.1A	40Ω

Chip Size 0.041″ × 0.043″

FERRANTI Power MOSFETS will directly interface with MICROPROCESSORS, LOGIC ARRAYS and standard IC LOGIC families including CMOS, TTL, PMOS and NMOS.

PACKAGE DIMENSIONS



PIN OUT	
1	Drain
2	Gate
3	Source

SYMBOL	INCHES		MILLIMETRES	
	MIN	MAX	MIN	MAX
A	.172	.188	4.37	4.77
B	.142	.158	3.61	4.01
C	.475	.525	12.06	13.34
D	.05		1.27	
E	.10		2.54	
F	.016	.019	.406	.495
G	.085	.095	2.16	2.42

Also available with various lead bends and on Tape and Reel.

ZVN0526A

ABSOLUTE MAXIMUM RATINGS

Parameters		ZVN0526A	Units
V_{DS}	Drain-source voltage	260	V
I_D	Continuous drain current (@ $T_A = 25°C$)	0.1	A
I_D	Continuous drain current (@ $T_C = 25°C$)	-	A
I_{DM}	Pulse drain current	0.6	A
V_{GS}	Gate-source voltage	±20	V
P_D	Max. Power Dissipation (@ $T_A = 25°C$)	0.70	W
P_D	Max. Power Dissipation (@ $T_C = 25°C$)	-	W
	Operating/Storage Temperature Range	−55 to +150	°C

ELECTRICAL CHARACTERISTICS (at T = 25°C unless otherwise stated)

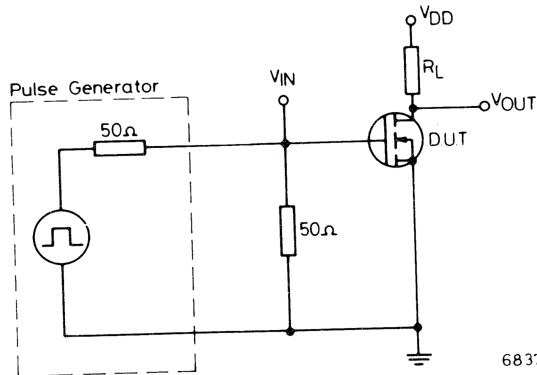
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Drain source breakdown voltage ZVN0526A	BV_{DSS}	260	-	-	V	$I_D = 1mA$, $V_{GS} = 0$
Gate-source threshold voltage	$V_{GS(th)}$	1	-	3	V	$I_D = 1mA$, $V_{DS} = V_{GS}$
Gate body leakage	I_{GSS}	-	-	20	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0$
Zero gate voltage Drain current (Note 2)	I_{DSS}	-	-	10	μA	V_{DS} = max. rating, $V_{GS} = 0$
		-	-	0.4	mA	$V_{DS} = 0.8 \times$ max. rating $V_{GS} = 0$ (T = 125°C)
On-state drain current*	$I_{D(ON)}$	0.15	0.25	-	A	$V_{DS} = 25V$, $V_{GS} = 10V$
Static drain-source ON-resistance*	$R_{DS(ON)}$	-	-	40	Ω	$I_D = 100mA$, $V_{GS} = 10V$
Forward transconductance* (Note 2)	g_{fs}	0.1	0.15	-	S	$V_{DS} = 25V$, $I_D = 0.1A$
Input capacitance (Note 2)	C_{iss}	-	54	70	pF	$V_{DS} = 25V$ $V_{GS} = 0$ f = 1MHz
Common source output capacitance (Note 2)	C_{oss}	-	5.1	10		
Reverse transfer capacitance (Note 2)	C_{rss}	-	1.4	4		
Turn-ON delay time (Notes 1 & 2)	$t_{d(on)}$	-	1.1	7	n secs	$V_{DD} = 25V$ $I_D = 0.1A$
Rise time (Notes 1 & 2)	t_r	-	1.8	7		
Turn-OFF delay time (Notes 1 & 2)	$t_{d(off)}$	-	8.5	16		
Fall time (Notes 1 & 2)	t_f	-	6.5	10		

*Measured under pulsed conditions. Width = 300μs. Duty cycle ≤ 2%.
Note 1 Switching times measured with 50 ohm source impedance and <5ns rise time on a pulse generator.
Note 2 Sample test.

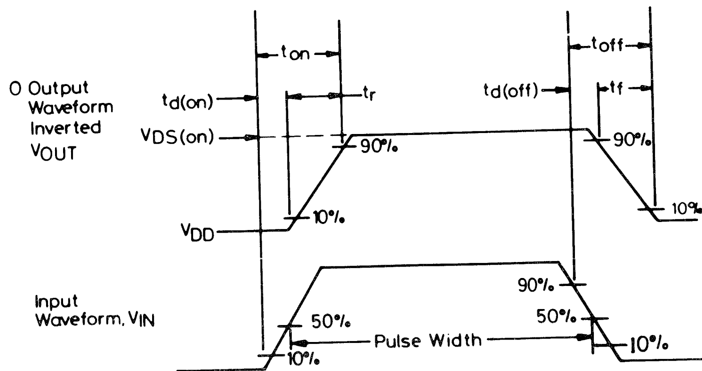
DRAIN-SOURCE DIODE CHARACTERISTICS

Parameter	Symbol	Typ.	Unit	Conditions
Forward ON voltage*	V_{SD}	0.74	V	$V_{GS}=0$, $I_S=90mA$

Circuit for Measuring Switching Times



Switching Waveforms



Input voltage amplitude 10 Volts peak

Note
Power MOSFET switching
times are essentially independent
of operating temperature

6838/1

Fig. 1 Output Characteristics

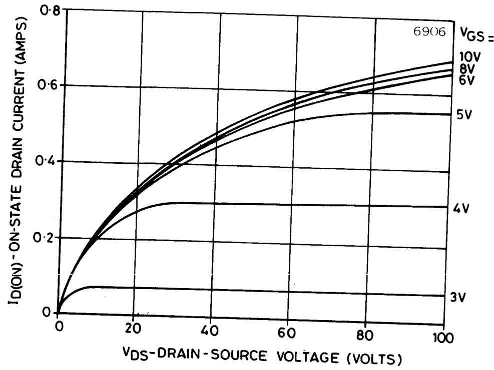


Fig. 2 Saturation Characteristics

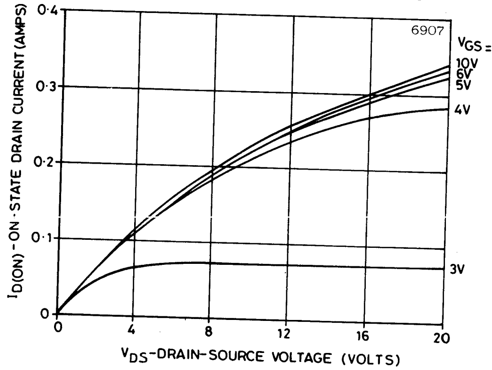


Fig. 3 Voltage Saturation Characteristics

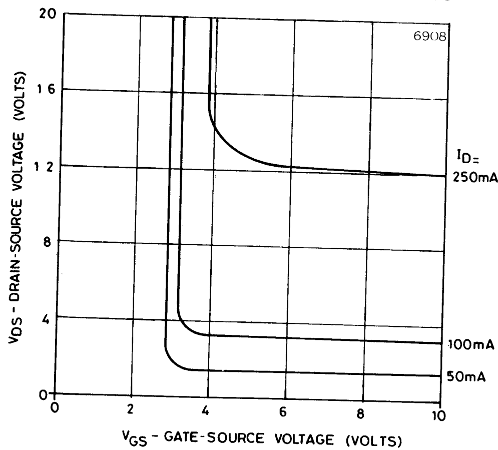


Fig. 4 Transfer Characteristics

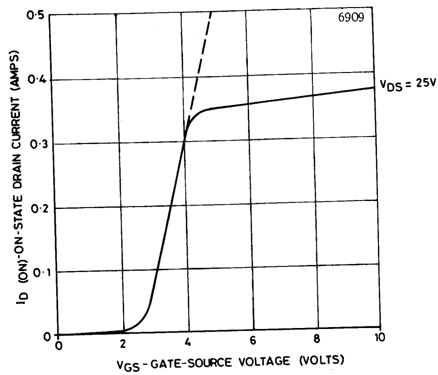


Fig. 5 Capacitance vs Drain-Source Voltage

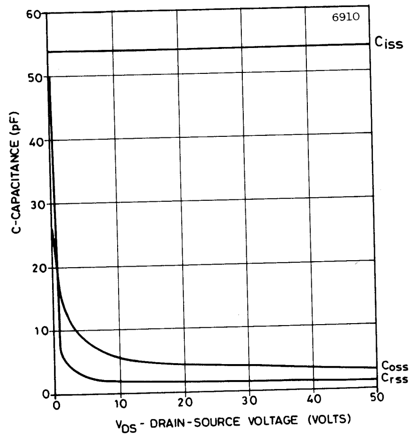


Fig. 6 Transconductance vs Drain Current

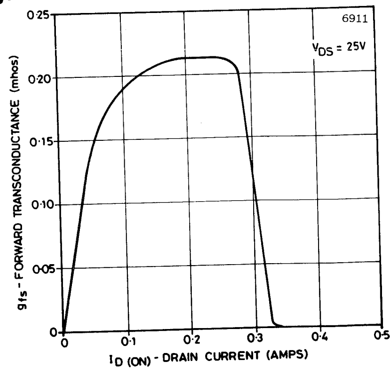


Fig. 7 Transconductance vs Gate-Source Voltage

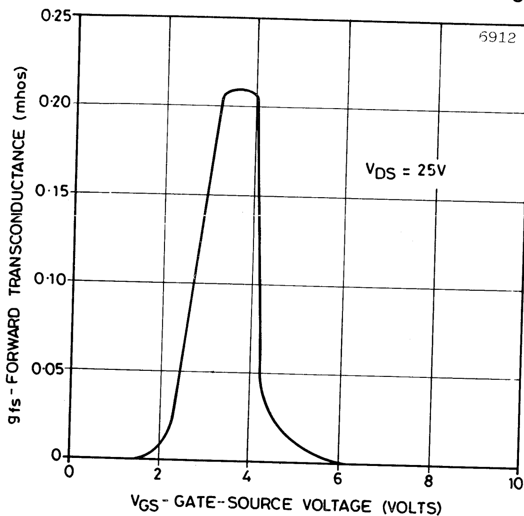


Fig. 8 Gate Charge vs Gate-Source Voltage

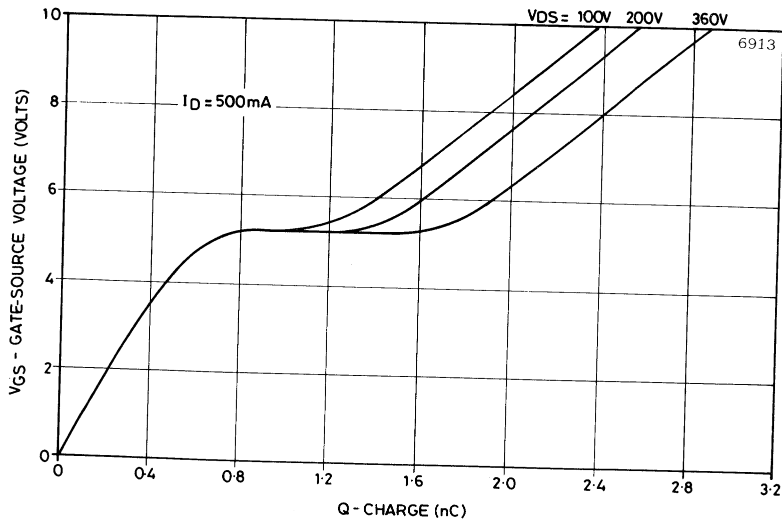


Fig. 9 ON-Resistance vs Gate-Source Voltage

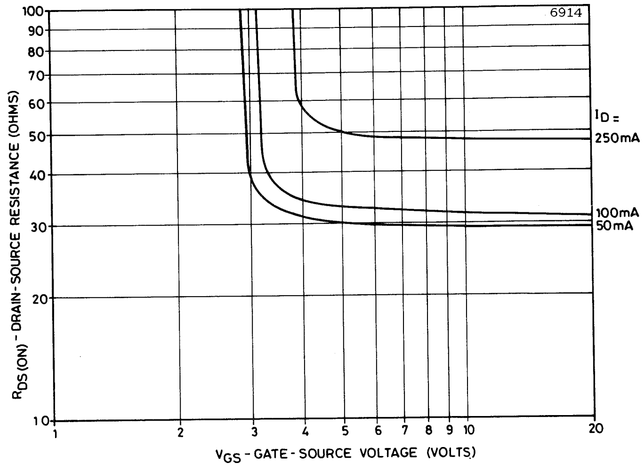
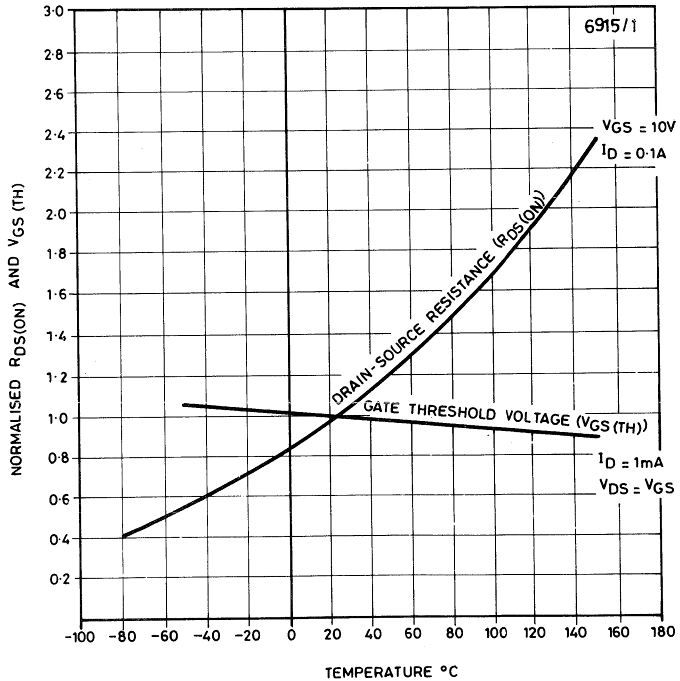
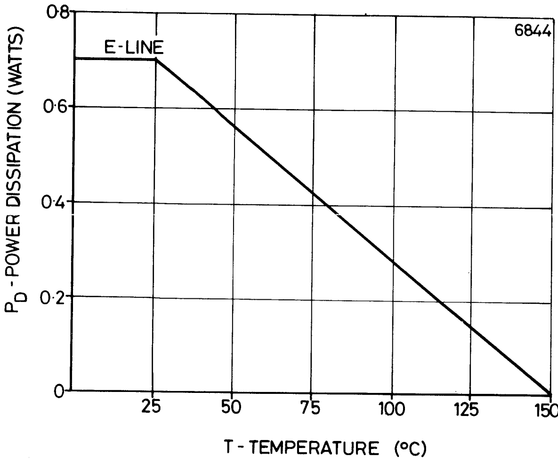


Fig. 10 Variation of $R_{DS(ON)}$ and $V_{GS(th)}$ with Temperature



ZVN0526A



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Issue 1, May 1984 4.5M

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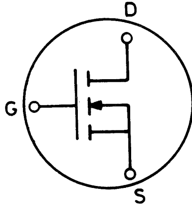
ZVN0530A
ZVN0535A

N-Channel Enhancement-Mode Vertical DMOS Power FET

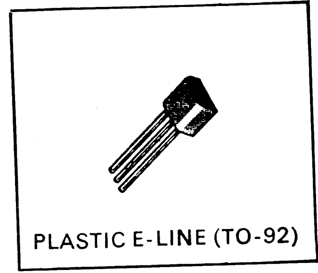
350V: 50 ohm: 90mA



N-Channel

FEATURES

- Compact Geometry
- Fast Switching Speeds
- No Secondary Breakdown
- Excellent Temperature Stability
- High Input Impedance
- Low Current Drive



PLASTIC E-LINE (TO-92)

DESCRIPTION

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The planar construction, coupled with ion implantation and the self-aligned poly-silicon gate manufacturing process, provides the reliability and stability in performance required in todays designs.

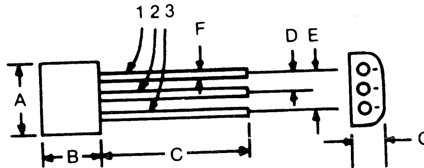
PRODUCT SUMMARY

Device Type	BV_{DSS}	$I_{D(CONT)}$	$R_{D(ON)}$
ZVN0530A	300V	0.09A	50Ω
ZVN0535A	350V	0.09A	50Ω

Chip Size 0.041″ × 0.043″

FERRANTI Power MOSFETS will directly interface with MICROPROCESSORS, LOGIC ARRAYS and standard IC LOGIC families including CMOS, TTL, PMOS and NMOS.

PACKAGE DIMENSIONS



PIN OUT	
1	Drain
2	Gate
3	Source

SYMBOL	INCHES		MILLIMETRES	
	MIN	MAX	MIN	MAX
A	.172	.188	4.37	4.77
B	.142	.158	3.61	4.01
C	.475	.525	12.06	13.34
D	.05		1.27	
E	.10		2.54	
F	.016	.019	.406	.495
G	.085	.095	2.16	2.42

Also available with various lead bends and on Tape and Reel.

ZVN0530A/0535A

ABSOLUTE MAXIMUM RATINGS

	Parameters	ZVN0530A	ZVN0535A	Units
V_{DS}	Drain-source voltage	300	350	V
I_D	Continuous drain current (@ $T_A = 25°C$)	0.09		A
I_D	Continuous drain current (@ $T_C = 25°C$)	-		A
I_{DM}	Pulse drain current	0.6		A
V_{GS}	Gate-source voltage	±20		V
P_D	Max. Power Dissipation (@ $T_A = 25°C$)	0.70		W
P_D	Max. Power Dissipation (@ $T_C = 25°C$)	-		W
	Operating/Storage Temperature Range	−55 to +150		°C

ELECTRICAL CHARACTERISTICS (at T=25°C unless otherwise stated)

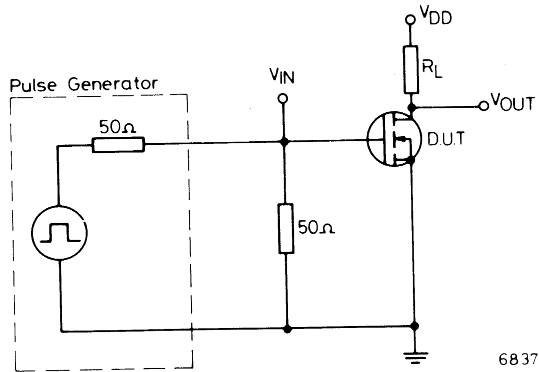
Parameter		Symbol	Min.	Typ.	Max.	Unit	Conditions
Drain source breakdown voltage	ZVN0530A	BV_{DSS}	300	-	-	V	$I_D = 1mA$, $V_{GS} = 0$
	ZVN0535A		350	-	-		
Gate-source threshold voltage		$V_{GS(th)}$	1	-	3	V	$I_D = 1mA$, $V_{DS} = V_{GS}$
Gate body leakage		I_{GSS}	-	-	20	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0$
Zero gate voltage Drain current (Note 2)		I_{DSS}	-	-	10	μA	V_{DS} = max. rating, $V_{GS} = 0$
			-	-	0.4	mA	$V_{DS} = 0.8 \times$ max. rating $V_{GS} = 0$ ($T = 125°C$)
On-state drain current*		$I_{D(ON)}$	0.15	0.25	-	A	$V_{DS} = 25V$, $V_{GS} = 10V$
Static drain-source ON-resistance*		$R_{DS(ON)}$	-	-	50	Ω	$I_D = 100mA$, $V_{GS} = 10V$
Forward transconductance* (Note 2)		g_{fs}	0.1	0.14	-	S	$V_{DS} = 25V$, $I_D = 0.1A$
Input capacitance (Note 2)		C_{iss}	-	54	70	pF	$V_{DS} = 25V$ $V_{GS} = 0$ f=1MHz
Common source output capacitance (Note 2)		C_{oss}	-	5.1	10		
Reverse transfer capacitance (Note 2)		C_{rss}	-	1.4	4		
Turn-ON delay time (Notes 1 & 2)		$t_{d(on)}$	-	1.1	7	n secs	$V_{DD} = 25V$ $I_D = 0.1A$
Rise time (Notes 1 & 2)		t_r	-	1.8	7		
Turn-OFF delay time (Notes 1 & 2)		$t_{d(off)}$	-	8.5	16		
Fall time (Notes 1 & 2)		t_f	-	6.5	10		

*Measured under pulsed conditions. Width=300μs. Duty cycle ≤2%.
Note 1 Switching times measured with 50 ohm source impedance and <5ns rise time on a pulse generator.
Note 2 Sample test.

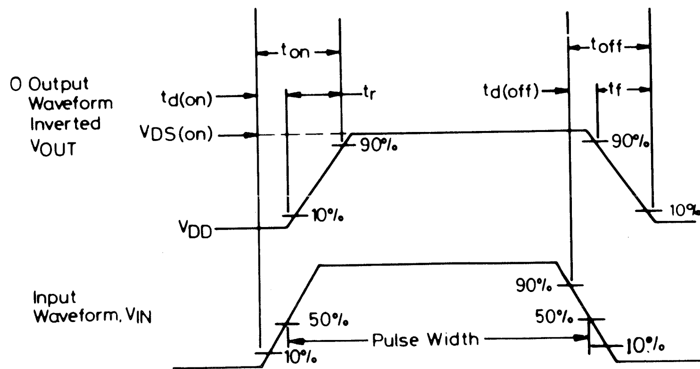
DRAIN-SOURCE DIODE CHARACTERISTICS

Parameter	Symbol	Typ.	Unit	Conditions
Forward ON voltage*	V_{SD}	0.74	V	$V_{GS}=0$, $I_S=90mA$

Circuit for Measuring Switching Times



Switching Waveforms



Note
Power MOSFET switching times are essentially independent of operating temperature

6838/1

Fig. 1 Output Characteristics

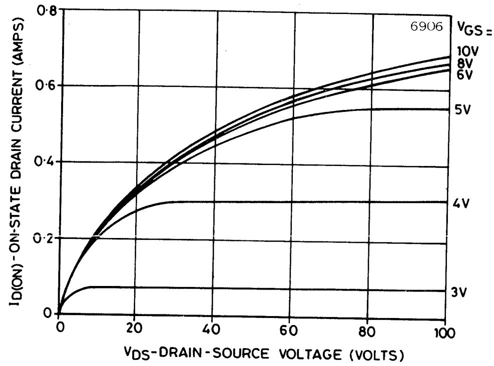


Fig. 2 Saturation Characteristics

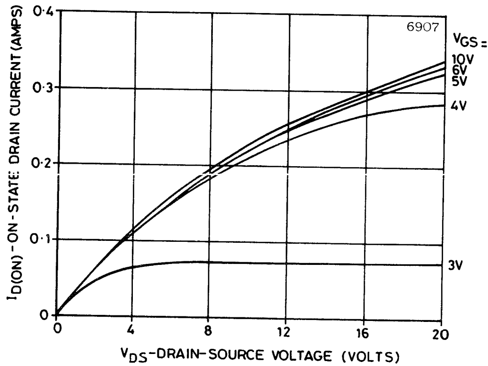


Fig. 3 Voltage Saturation Characteristics

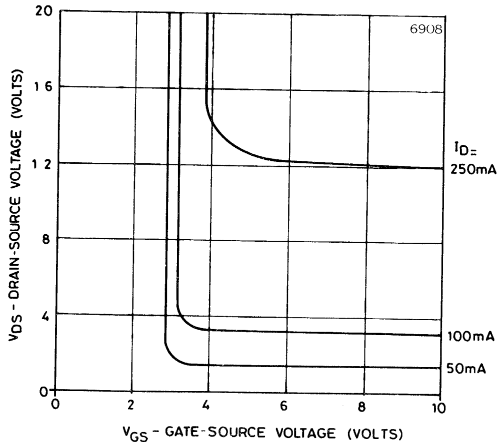


Fig. 4 Transfer Characteristics

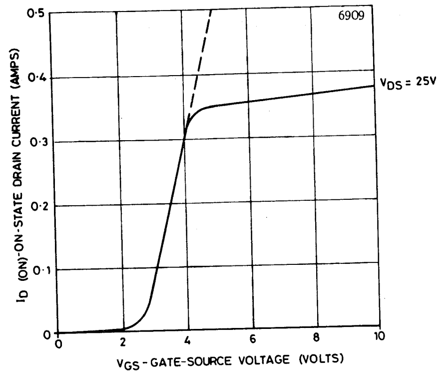


Fig. 5 Capacitance vs Drain-Source Voltage

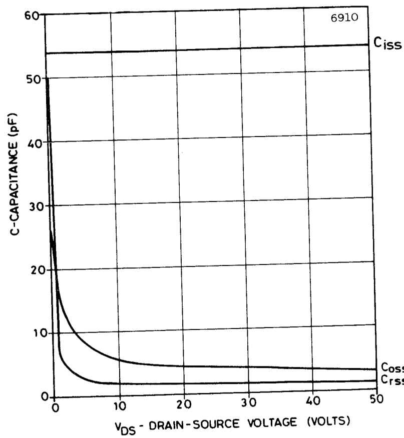


Fig. 6 Transconductance vs Drain Current

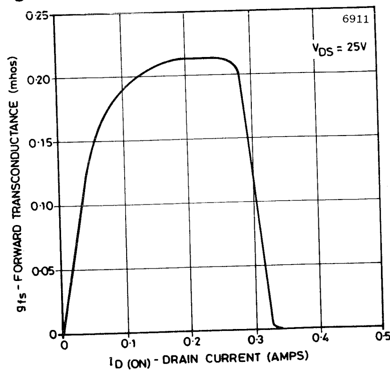


Fig. 7 Transconductance vs Gate-Source Voltage

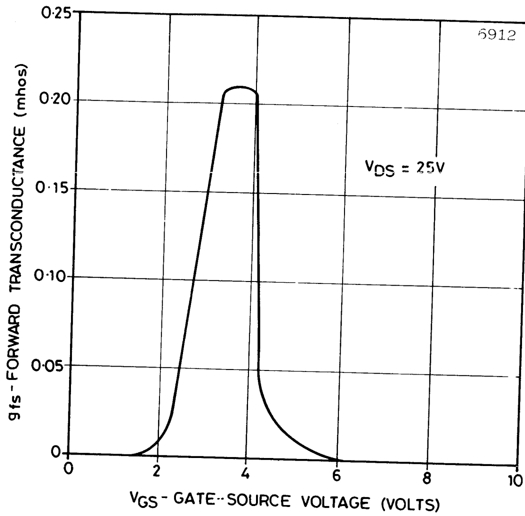


Fig. 8 Gate Charge vs Gate-Source Voltage

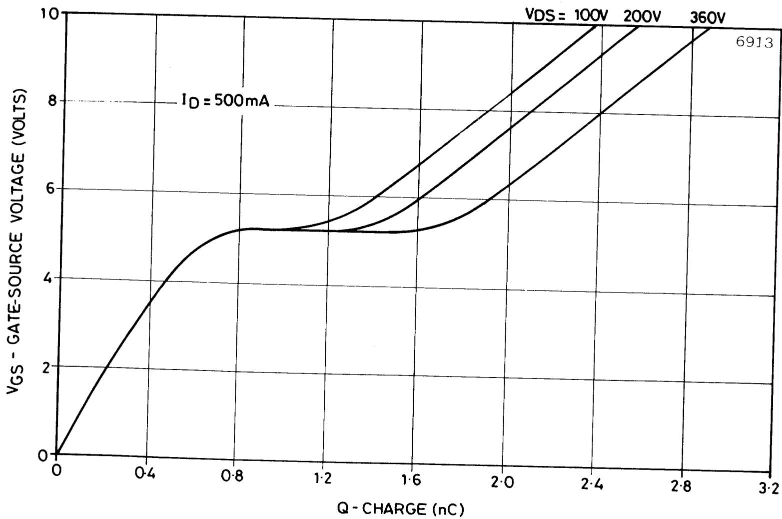


Fig. 9 ON-Resistance vs Gate-Source Voltage

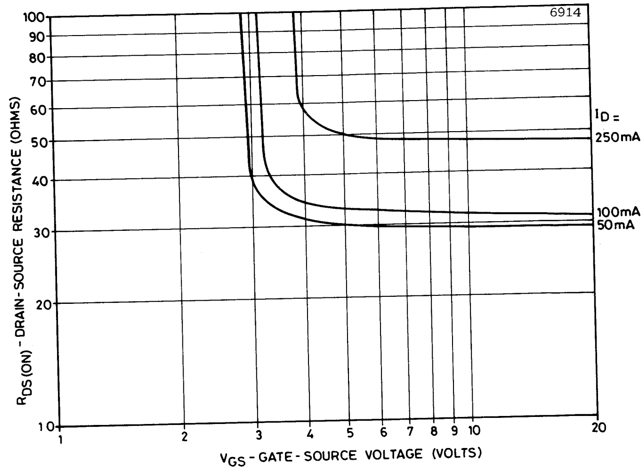
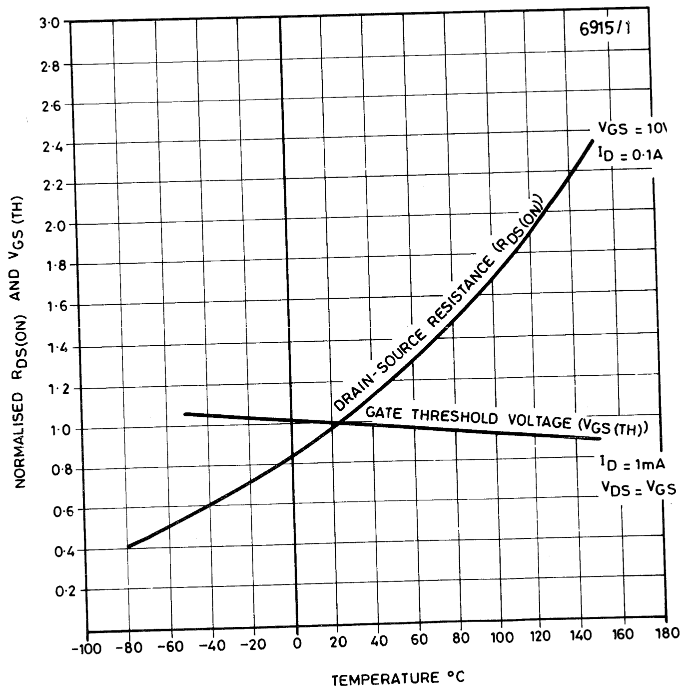
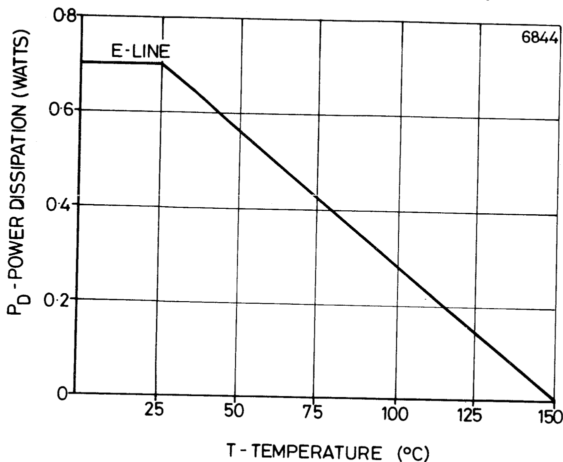


Fig. 10 Variation of $R_{DS(ON)}$ and $V_{GS(th)}$ with Temperature



ZVN0530A/0535A

Fig. 11 Power Derating (Ambient)



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Tel: 408-438 2900 TWX: 910 598 4513

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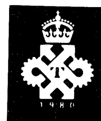
Gee Chang Hong Centre, Aberdeen, Hong Kong Tel: 5-538298-9 Telex: HX 74605

Issue 1, May 1984 4.5M

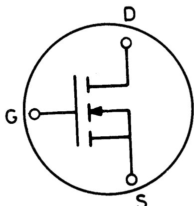


ZVN0530B
ZVN0535B

FERRANTI semiconductors ®

N-Channel Enhancement-Mode Vertical DMOS Power FET

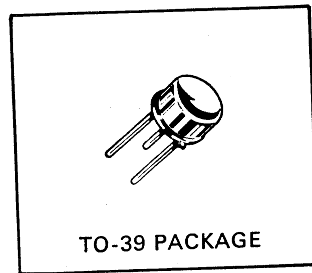
350V: 50 ohm: 0.15A



N-Channel

FEATURES

- Compact Geometry
- Fast Switching Speeds
- No Secondary Breakdown
- Excellent Temperature Stability
- High Input Impedance
- Low Current Drive



TO-39 PACKAGE

DESCRIPTION

Compact OVERLAY (CELL) and INTER-DIGITATED geometries are the basis of the new generation of FERRANTI Power MOSFET transistors. These efficient geometries, optimised for low ON-resistance, low capacitances and fast switching speeds, with computer controlled processing combine to achieve greater device ruggedness.

The planar construction, coupled with ion implantation and the self-aligned poly-silicon gate manufacturing process, provides the reliability and stability in performance required in todays designs.

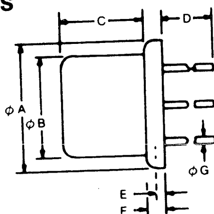
PRODUCT SUMMARY

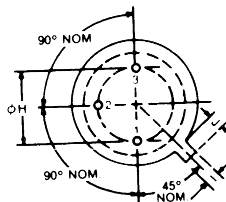
Device Type	BV_{DSS}	$I_{D(CONT)}$	$R_{D(ON)}$
ZVN0530B	300V	0.15A	50Ω
ZVN0535B	350V	0.15A	50Ω

Chip Size 0.041" × 0.043"

FERRANTI Power MOSFETS will directly interface with MICROPROCESSORS, LOGIC ARRAYS and standard IC LOGIC families including CMOS, TTL, PMOS and NMOS.

PACKAGE DIMENSIONS





PIN OUT	
1	Source
2	Gate
3	Drain & Case

SYMBOL	INCHES		MILLIMETRES	
	MIN	MAX	MIN	MAX
φA	.350	.370	8.89	9.40
φB	.306	.335	7.77	8.51
C	.240	.260	6.10	6.60
D	.500		12.70	
E	.009	.023	.229	.584
F	.018	.045	.458	1.143
φG	.016	.021	.406	.533
φH	.190	.210	4.83	5.33
I	.028	.037	.711	.939
J	.026	.040	.660	1.016

ZVN0530B/0535B

ABSOLUTE MAXIMUM RATINGS

Parameters		ZVN0530B	ZVN0535B	Units
V_{DS}	Drain-source voltage	300	350	V
I_D	Continuous drain current (@ $T_A = 25°C$)	0.09		A
I_D	Continuous drain current (@ $T_C = 25°C$)	0.15		A
I_{DM}	Pulse drain current	0.60		A
V_{GS}	Gate-source voltage	±20		V
P_D	Max. Power Dissipation (@ $T_A = 25°C$)	0.70		W
P_D	Max. Power Dissipation (@ $T_C = 25°C$)	5		W
	Operating/Storage Temperature Range	−55 to +150		°C

ELECTRICAL CHARACTERISTICS (at T=25°C unless otherwise stated)

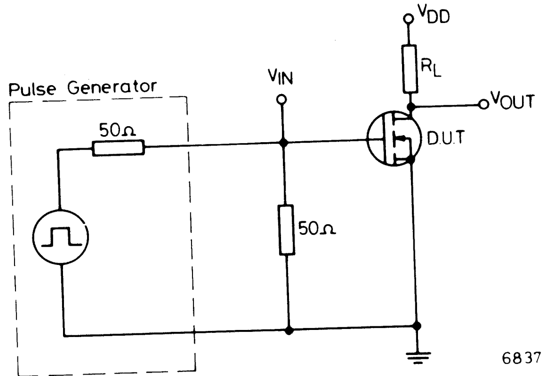
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Drain source breakdown voltage ZVN0530B	BV_{DSS}	300	-	-	V	$I_D = 1mA$, $V_{GS} = 0$
Drain source breakdown voltage ZVN0535B		350	-	-		
Gate-source threshold voltage	$V_{GS(th)}$	1	-	3	V	$I_D = 1mA$, $V_{DS} = V_{GS}$
Gate body leakage	I_{GSS}	-	-	20	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0$
Zero gate voltage Drain current (Note 2)	I_{DSS}	-	-	10	μA	V_{DS} = max. rating, $V_{GS} = 0$
		-	-	0.4	mA	$V_{DS} = 0.8 \times$ max. rating $V_{GS} = 0$ ($T = 125°C$)
On-state drain current*	$I_{D(ON)}$	0.15	0.25	-	A	$V_{DS} = 25V$, $V_{GS} = 10V$
Static drain-source ON-resistance*	$R_{DS(ON)}$	-	-	50	Ω	$I_D = 100mA$, $V_{GS} = 10V$
Forward transconductance* (Note 2)	g_{fs}	0.1	0.14	-	S	$V_{DS} = 25V$, $I_D = 0.1A$
Input capacitance (Note 2)	C_{iss}	-	54	70	pF	$V_{DS} = 25V$ $V_{GS} = 0$ f=1MHz
Common source output capacitance (Note 2)	C_{oss}	-	5.1	10		
Reverse transfer capacitance (Note 2)	C_{rss}	-	1.4	4		
Turn-ON delay time (Notes 1 & 2)	$t_{d(on)}$	-	1.1	7	n secs	$V_{DD} = 25V$ $I_D = 0.1A$
Rise time (Notes 1 & 2)	t_r	-	1.8	7		
Turn-OFF delay time (Notes 1 & 2)	$t_{d(off)}$	-	8.5	16		
Fall time (Notes 1 & 2)	t_f	-	6.5	10		

*Measured under pulsed conditions. Width=300μs. Duty cycle ≤2%.
Note 1 Switching times measured with 50 ohm source impedance and <5ns rise time on a pulse generator.
Note 2 Sample test.

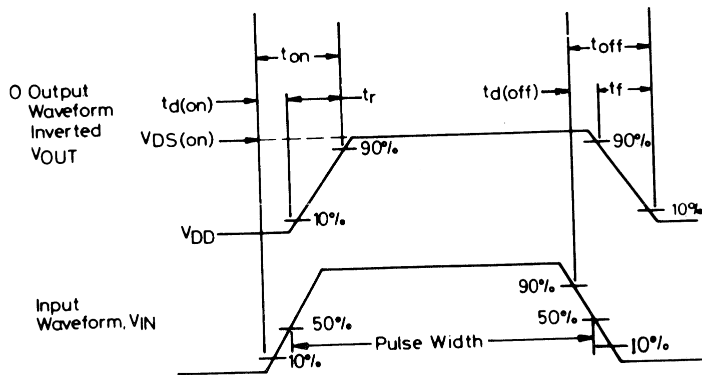
DRAIN-SOURCE DIODE CHARACTERISTICS

Parameter	Symbol	Typ.	Unit	Conditions
Forward ON voltage*	V_{SD}	0.74	V	$V_{GS}=0$, $I_S=150mA$

Circuit for Measuring Switching Times



Switching Waveforms



Input voltage amplitude 10 Volts peak

Note:
Power MOSFET switching times are essentially independent of operating temperature

6838/1

ZVN0530B/0535B

Fig. 1 Output Characteristics

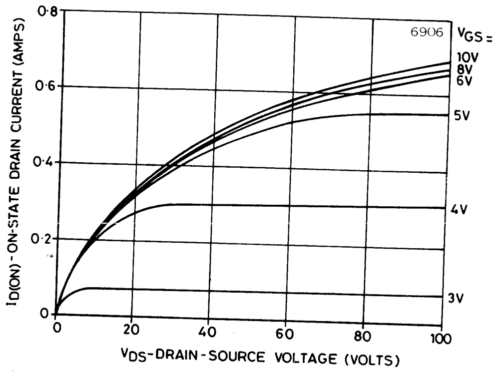


Fig. 2 Saturation Characteristics

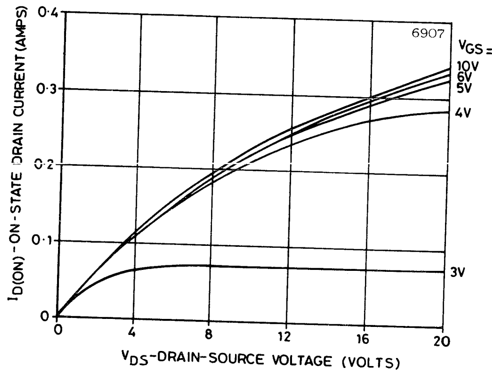


Fig. 3 Voltage Saturation Characteristics

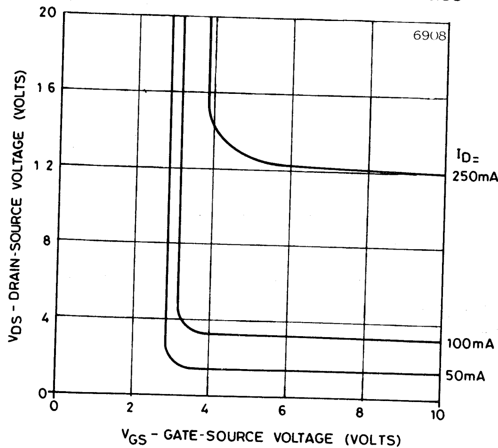


Fig. 4 Transfer Characteristics

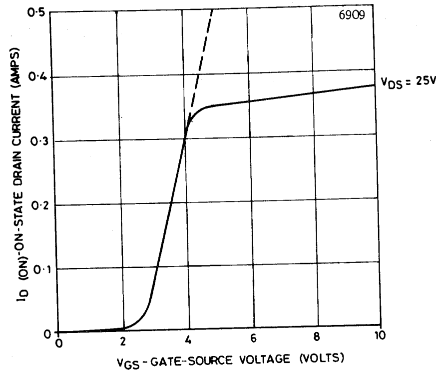


Fig. 5 Capacitance vs Drain-Source Voltage

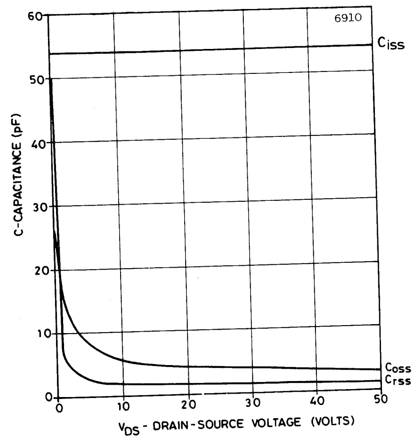
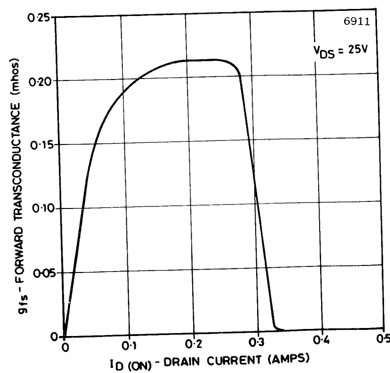


Fig. 6 Transconductance vs Drain Current



ZVN0530B/0535B

Fig. 7 Transconductance vs Gate-Source Voltage

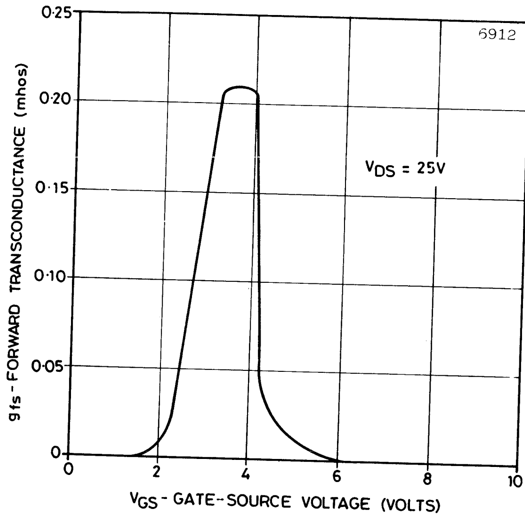


Fig. 8 Gate Charge vs Gate-Source Voltage

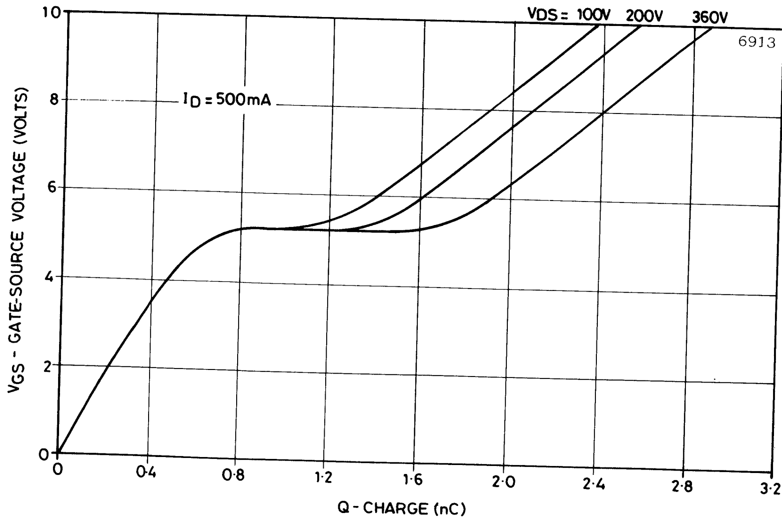


Fig. 9 ON-Resistance vs Gate-Source Voltage

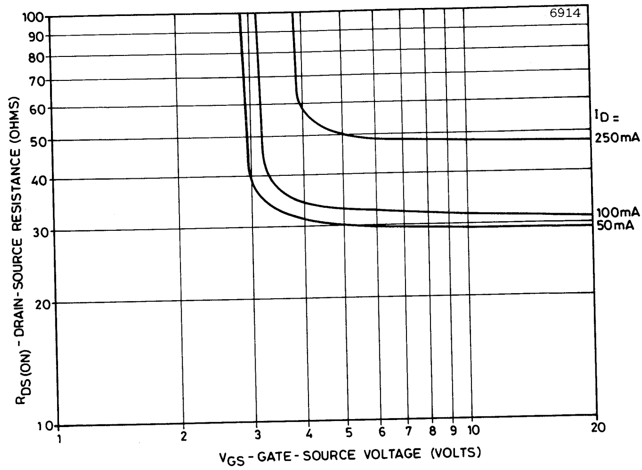


Fig. 10 Variation of $R_{DS(ON)}$ and $V_{GS(th)}$ with Temperature

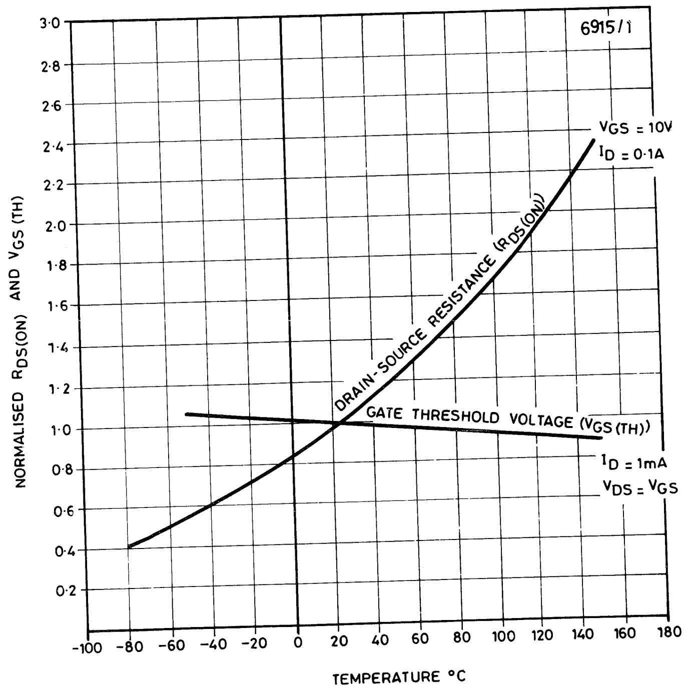


Fig. 11 Power Derating (Case)

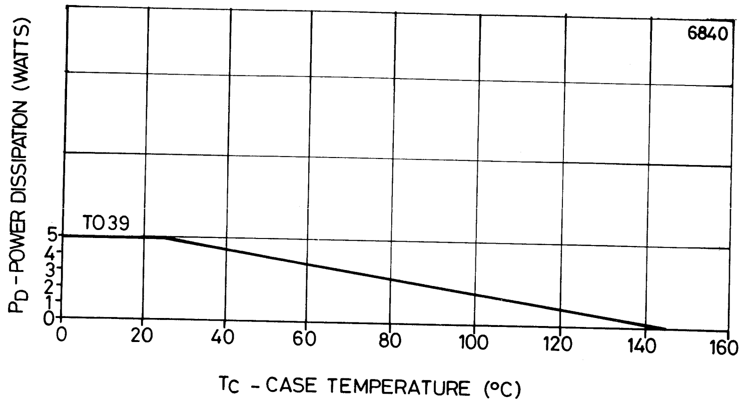
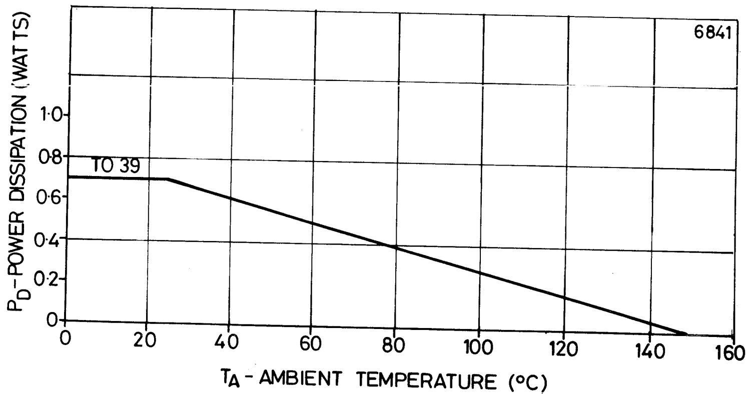


Fig. 12 Power Derating (Ambient)



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Tel: 408-438 2900 TWX: 910 598 4513
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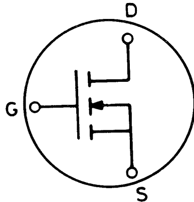
Issue 1, May 1984 4.5M

FERRANTI semiconductors ®

ZVN0530L ZVN0535L

N-Channel Enhancement-Mode Vertical DMOS Power FET

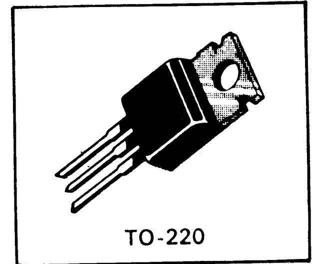
350V: 50 ohm: 0.15A



N-Channel

FEATURES

- Compact Geometry
- Fast Switching Speeds
- No Secondary Breakdown
- Excellent Temperature Stability
- High Input Impedance
- Low Current Drive



TO-220

DESCRIPTION

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The planar construction, coupled with ion implantation and the self-aligned poly-silicon gate manufacturing process, provides the reliability and stability in performance required in todays designs.

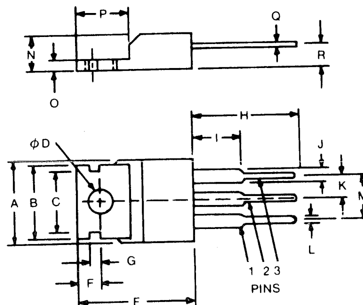
PRODUCT SUMMARY

Device Type	BV_{DSS}	$I_{D(CONT)}$	$R_{D(ON)}$
ZVN0530L	300V	0.15A	50Ω
ZVN0535L	350V	0.15A	50Ω

Chip Size 0.041″ × 0.043″

FERRANTI Power MOSFETS will directly interface with MICROPROCESSORS, LOGIC ARRAYS and standard IC LOGIC families including CMOS, TTL, PMOS and NMOS.

PACKAGE DIMENSIONS



PIN OUT	
1	Gate
2	Drain & Tab
3	Source

SYMBOL	INCHES		MILLIMETRES	
	MIN	MAX	MIN	MAX
A	.380	.420	9.65	10.66
B	.380	.420	9.65	10.66
C	.300	.320	7.62	8.12
φD	.139	.147	3.531	3.733
E	.560	.625	14.230	15.870
F	.100	.120	2.54	3.04
G	.040	.060	1.02	1.52
H	.500	.562	12.70	14.27
I		.250		6.35
J	.045	.060	1.14	1.52
K	.090	.110	2.29	2.79
L	.020	.040	.510	1.016
M	.190	.210	4.830	5.330
N	.175	.185	4.445	4.699
O	.030	.055	.762	1.390
P	.230	.270	5.850	6.850
Q	.015	.025	.380	.630
R	.080	.115	2.040	2.920

ZVN0530L/0535L

ABSOLUTE MAXIMUM RATINGS

	Parameters	ZVN0530L	ZVN0535L	Units
V_{DS}	Drain-source voltage	300	350	V
I_D	Continuous drain current (@ $T_A = 25°C$)	0.13		A
I_D	Continuous drain current (@ $T_C = 25°C$)	0.15		A
I_{DM}	Pulse drain current	0.60		A
V_{GS}	Gate-source voltage	±20		V
P_D	Max. Power Dissipation (@ $T_A = 25°C$)	1.50		W
P_D	Max. Power Dissipation (@ $T_C = 25°C$)	20		W
	Operating/Storage Temperature Range	−55 to +150		°C

ELECTRICAL CHARACTERISTICS (at T = 25°C unless otherwise stated)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Drain source breakdown voltage ZVN0530L	BV_{DSS}	300	-	-	V	$I_D = 1mA$, $V_{GS} = 0$
Drain source breakdown voltage ZVN0535L		350	-	-		
Gate-source threshold voltage	$V_{GS(th)}$	1	-	3	V	$I_D = 1mA$, $V_{DS} = V_{GS}$
Gate body leakage	I_{GSS}	-	-	20	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0$
Zero gate voltage Drain current (Note 2)	I_{DSS}	-	-	10	μA	V_{DS} = max. rating, $V_{GS} = 0$
		-	-	0.4	mA	$V_{DS} = 0.8 \times$ max. rating $V_{GS} = 0$ (T = 125°C)
On-state drain current*	$I_{D(ON)}$	0.15	0.25	-	A	$V_{DS} = 25V$, $V_{GS} = 10V$
Static drain-source ON-resistance*	$R_{DS(ON)}$	-	-	50	Ω	$I_D = 100mA$, $V_{GS} = 10V$
Forward transconductance* (Note 2)	g_{fs}	0.1	0.14	-	S	$V_{DS} = 25V$, $I_D = 0.1A$
Input capacitance (Note 2)	C_{iss}	-	54	70	pF	$V_{DS} = 25V$ $V_{GS} = 0$ f = 1MHz
Common source output capacitance (Note 2)	C_{oss}	-	5.1	10		
Reverse transfer capacitance (Note 2)	C_{rss}	-	1.4	4		
Turn-ON delay time (Notes 1 & 2)	$t_{d(on)}$	-	1.1	7	n secs	$V_{DD} = 25V$ $I_D = 0.1A$
Rise time (Notes 1 & 2)	t_r	-	1.8	7		
Turn-OFF delay time (Notes 1 & 2)	$t_{d(off)}$	-	8.5	16		
Fall time (Notes 1 & 2)	t_f	-	6.5	10		

*Measured under pulsed conditions. Width = 300μs. Duty cycle ≤2%.

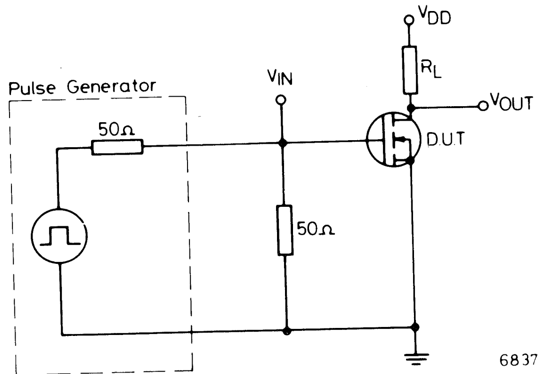
Note 1 Switching times measured with 50 ohm source impedance and <5ns rise time on a pulse generator.

Note 2 Sample test.

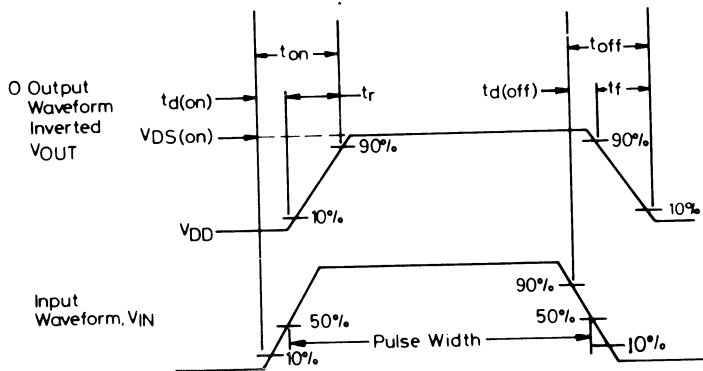
DRAIN-SOURCE DIODE CHARACTERISTICS

Parameter	Symbol	Typ.	Unit	Conditions
Forward ON voltage*	V_{SD}	0.74	V	$V_{GS}=0$, $I_S=150mA$

Circuit for Measuring Switching Times



Switching Waveforms



Input voltage amplitude 10 Volts peak

Note
Power MOSFET switching times are essentially independent of operating temperature

6838/1

ZVN0530L/0535L

Fig. 1 Output Characteristics

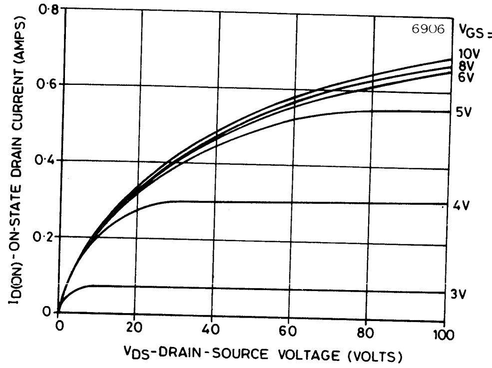


Fig. 2 Saturation Characteristics

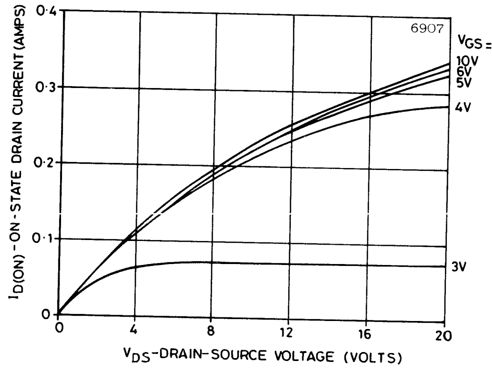


Fig. 3 Voltage Saturation Characteristics

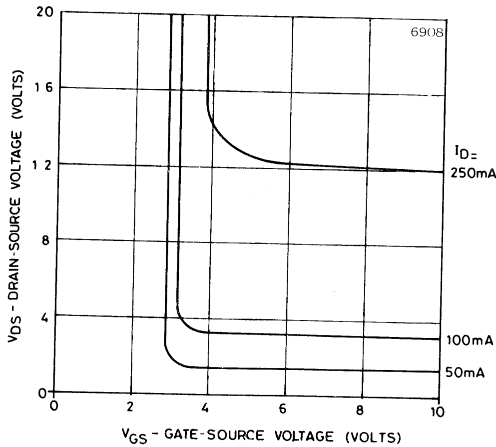


Fig. 4 Transfer Characteristics

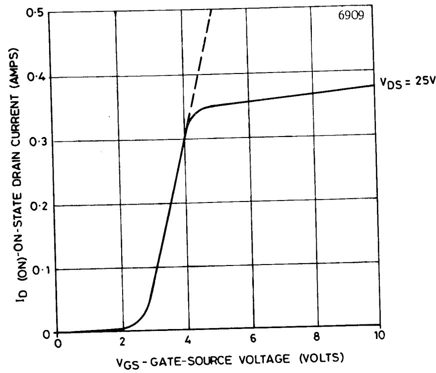


Fig. 5 Capacitance vs Drain-Source Voltage

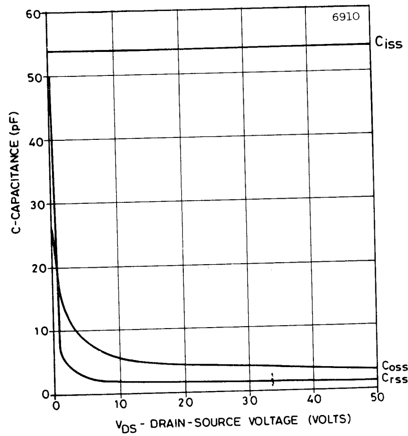


Fig. 6 Transconductance vs Drain Current

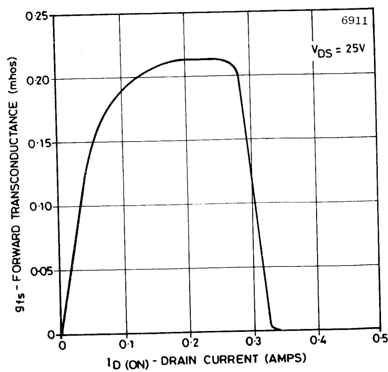


Fig. 7 Transconductance vs Gate-Source Voltage

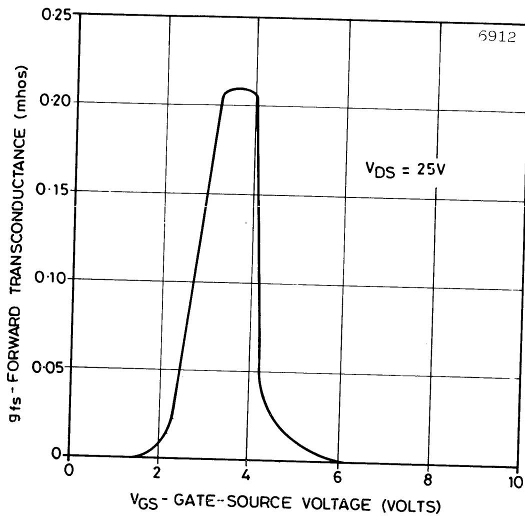


Fig. 8 Gate Charge vs Gate-Source Voltage

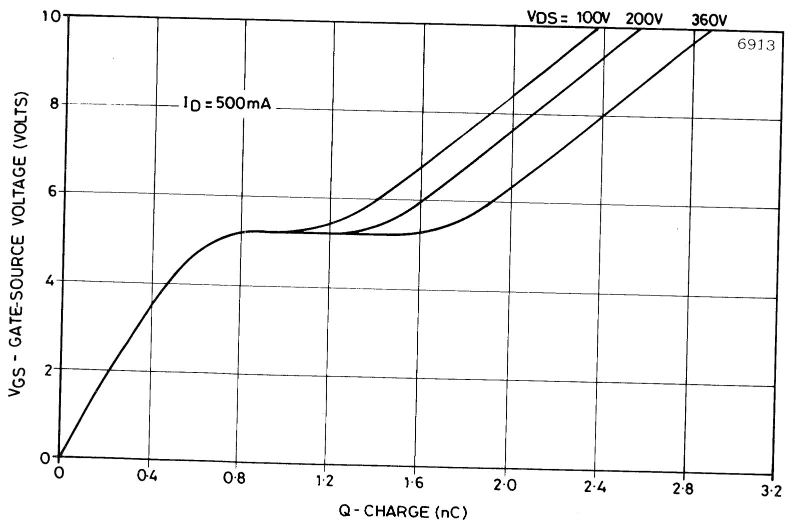


Fig. 9 ON-Resistance vs Gate-Source Voltage

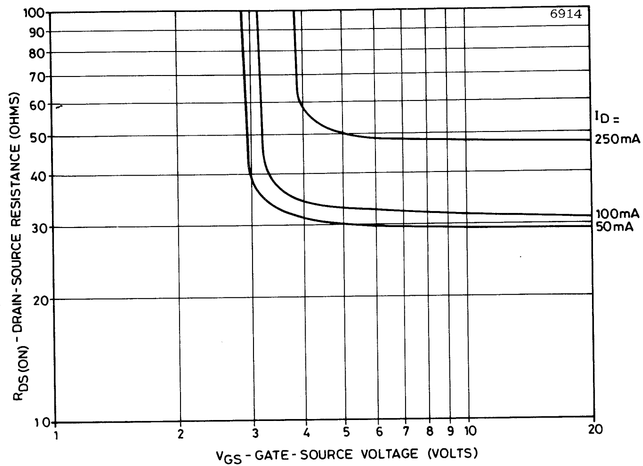
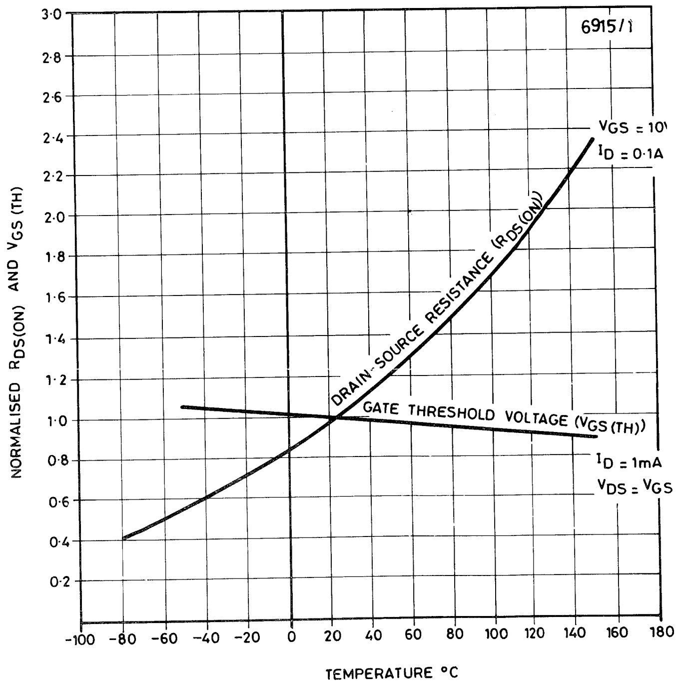


Fig. 10 Variation of $R_{DS(ON)}$ and $V_{GS(th)}$ with Temperature



ZVN0530L/0535L

Fig. 11 Power Derating (Case)

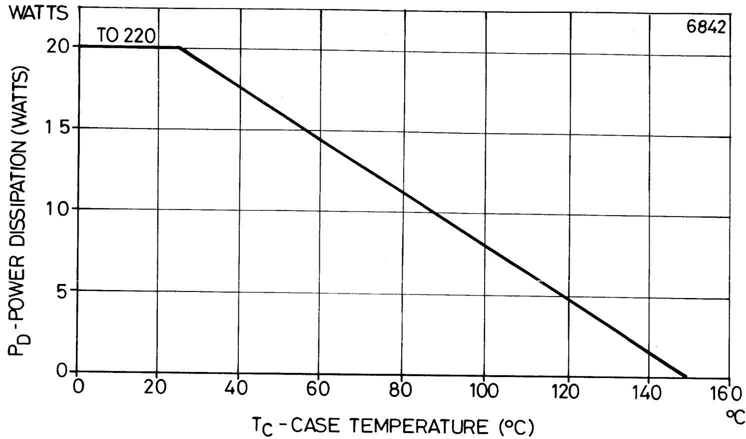
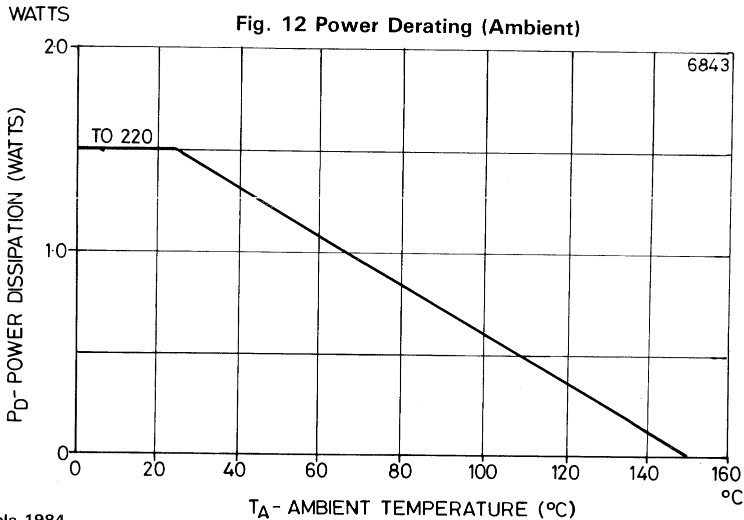


Fig. 12 Power Derating (Ambient)



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Issue 1, May 1984 4.5M

Printed in England CP

Section 5

ZVN33 Range

ZVN3306A/B

ZVN3310A/B

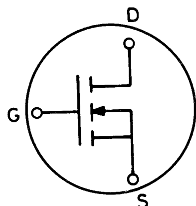
ZVN1320A/B

ZVN3302A
ZVN3304A
ZVN3306A

FERRANTI semiconductors ®

N-Channel Enhancement-Mode Vertical DMOS Power FET

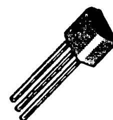
60V: 5 ohm: 0.27A



N-Channel

FEATURES

- Compact Geometry
- Fast Switching Speeds
- No Secondary Breakdown
- Excellent Temperature Stability
- High Input Impedance
- Low Current Drive
- Ease of Paralleling



PLASTIC E-LINE (TO-92)

DESCRIPTION

Compact OVERLAY (CELL) and INTER-DIGITATED geometries are the basis of the new generation of FERRANTI Power MOSFET transistors. These efficient geometries, optimised for low ON-resistance, low capacitances and fast switching speeds, with computer controlled processing combine to achieve greater device ruggedness.

The planar construction, coupled with ion implantation and the self-aligned poly-silicon gate manufacturing process, provides the reliability and stability in performance required in todays designs.

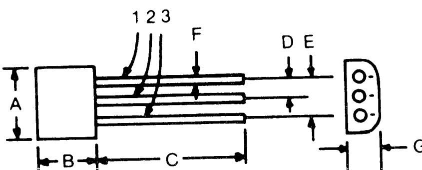
PRODUCT SUMMARY

Device Type	BV_{DSS}	$I_{D(CONT)}$	$R_{D(ON)}$
ZVN3302A	20V	0.27A	5Ω
ZVN3304A	40V	0.27A	5Ω
ZVN3306A	60V	0.27A	5Ω

Chip Size 0.030″ × 0.030″

FERRANTI Power MOSFETS will directly interface with MICROPROCESSORS, LOGIC ARRAYS and standard IC LOGIC families including CMOS, TTL, PMOS and NMOS.

PACKAGE DIMENSIONS



PIN OUT	
1	Drain
2	Gate
3	Source

SYMBOL	INCHES		MILLIMETRES	
	MIN	MAX	MIN	MAX
A	.172	.188	4.37	4.77
B	.142	.158	3.61	4.01
C	.475	.525	12.06	13.34
D	.05		1.27	
E	.10		2.54	
F	.016	.019	.406	.495
G	.085	.095	2.16	2.42

Also available with various lead bends and on Tape and Reel

ZVN3302A/3304A/3306A

ABSOLUTE MAXIMUM RATINGS

	Parameters	ZVN3302A	ZVN3304A	ZVN3306A	Units
V_{DS}	Drain-source voltage	20	40	60	V
I_D	Continuous drain current (@ $T_A = 25°C$)	0.27			A
I_D	Continuous drain current (@ $T_C = 25°C$)	-			A
I_{DM}	Pulse drain current	3			A
V_{GS}	Gate-source voltage	±20			V
P_D	Max. power dissipation (@ $T_A = 25°C$)	0.625			W
P_D	Max. power dissipation (@ $T_C = 25°C$)	-			W
	Operating/Storage Temperature Range	−55 to +150			°C

ELECTRICAL CHARACTERISTICS (at T = 25°C unless otherwise stated)

Parameter		Symbol	Min.	Typ.	Max.	Unit	Conditions
Drain source breakdown voltage	ZVN3302A	BV_{DSS}	20	-	-	V	$I_D = 1mA$
	ZVN3304A		40	-	-		
	ZVN3306A		60	-	-		$V_{GS} = 0$
Gate-source threshold voltage		$V_{GS(th)}$	0.8	-	2.4	V	$I_D = 1mA$, $V_{DS} = V_{GS}$
Gate body leakage		I_{GSS}	-	0.1	20	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0$
Zero gate voltage Drain current		I_{DSS}	-	-	0.5	μA	V_{DS} = max. rating, $V_{GS} = 0$
(Note 2)			-	-	0.05	mA	$V_{DS} = 0.8 \times$ max. rating $V_{GS} = 0$ ($T = 125°C$)
On-state drain current*		$I_{D(ON)}$	0.75	1.5	-	A	$V_{DS} = 18V$, $V_{GS} = 10V$
Static drain-source ON-resistance*		$R_{DS(ON)}$	-	4	5	Ω	$I_D = 0.5A$, $V_{GS} = 10V$
Forward transconductance* (Note 2)		g_{fs}	0.15	0.18	-	S	$V_{DS} = 18V$, $I_D = 0.5A$
Input capacitance (Note 2)		C_{iss}	-	31	35	pF	$V_{DS} = 18V$
Common source output capacitance (Note 2)		C_{oss}	-	11	25		$V_{GS} = 0$
Reverse transfer capacitance (Note 2)		C_{rss}	-	3	8		f = 1MHz
Turn-ON delay time (Notes 1 & 2)		$t_{d(on)}$	-	3	5	n secs	$V_{DD} = 18V$
Rise time (Notes 1 & 2)		t_r	-	4	7		
Turn-OFF delay time (Notes 1 & 2)		$t_{d(off)}$	-	4	6		$I_D = 0.5A$
Fall time (Notes 1 & 2)		t_f	-	5	8		

*Measured under pulsed conditions. Width = 300μs. Duty cycle ≤ 2%.

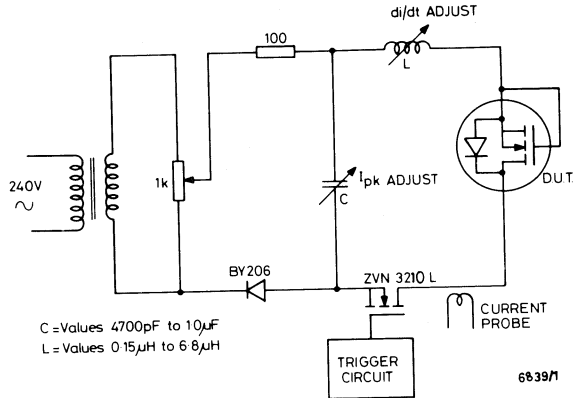
Note 1 Switching times measured with 50 ohm source impedance and <5ns rise time on a pulse generator.

Note 2 Sample test.

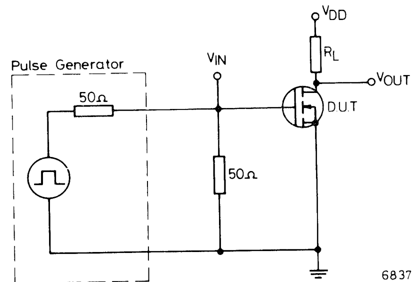
DRAIN-SOURCE DIODE CHARACTERISTICS

Parameter	Symbol	Typ.	Unit	Conditions
Forward ON voltage*	V_{SD}	0.85	V	$V_{GS}=0$, $I_S=270mA$
Reverse recovery time	t_{rr}	90	n secs	$V_{GS}=0$, $I_F=270mA$, $I_R=100mA$

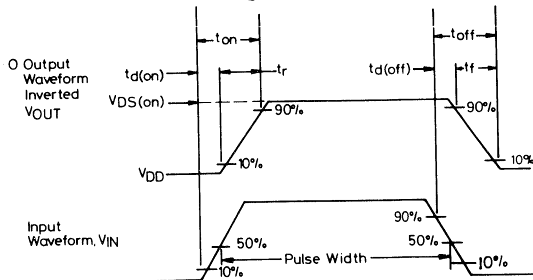
Reverse Recovery Test Circuit



Circuit for Measuring Switching Times



Switching Waveforms



Note:
Power MOSFET switching times are essentially independent of operating temperature

Fig. 1 Saturation Characteristics

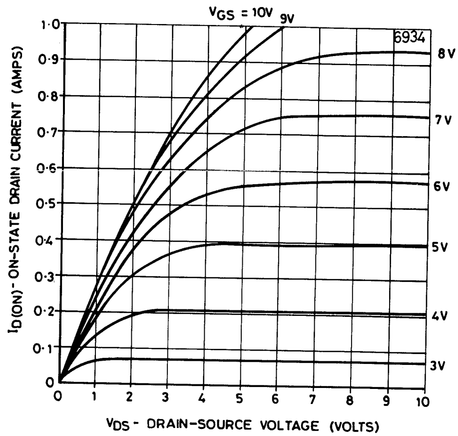


Fig. 2 Voltage Saturation Characteristics

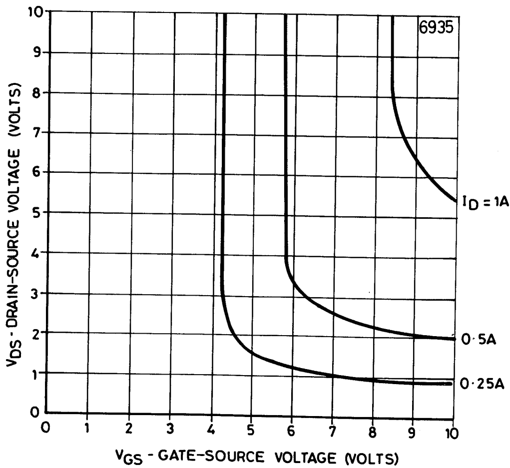


Fig. 3 Transfer Characteristics

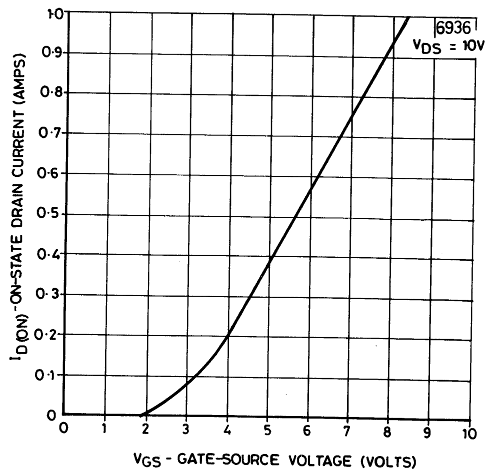


Fig. 4 Capacitance vs Drain-Source Voltage

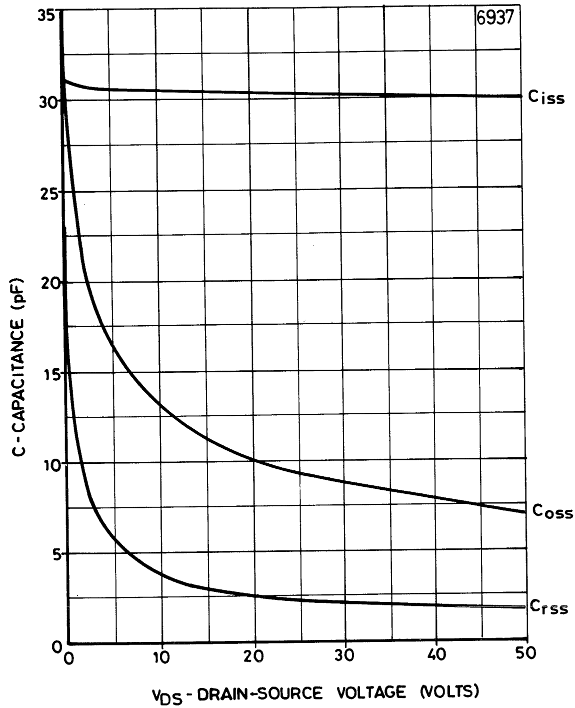


Fig. 5 Transconductance vs Drain-Current

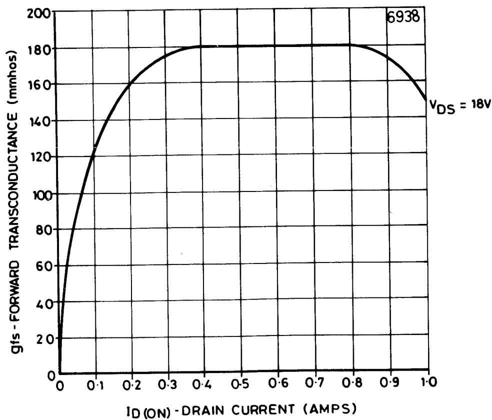


Fig. 6 Transconductance vs Gate-Source Voltage

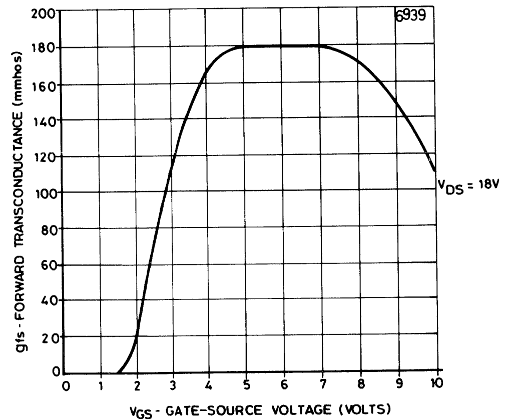


Fig. 7 Gate Charge vs Gate-Source Voltage

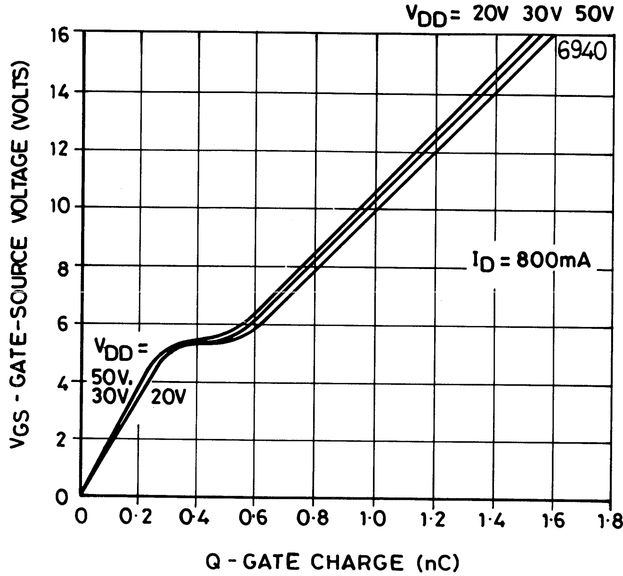


Fig. 8 ON-Resistance vs Gate-Source Voltage

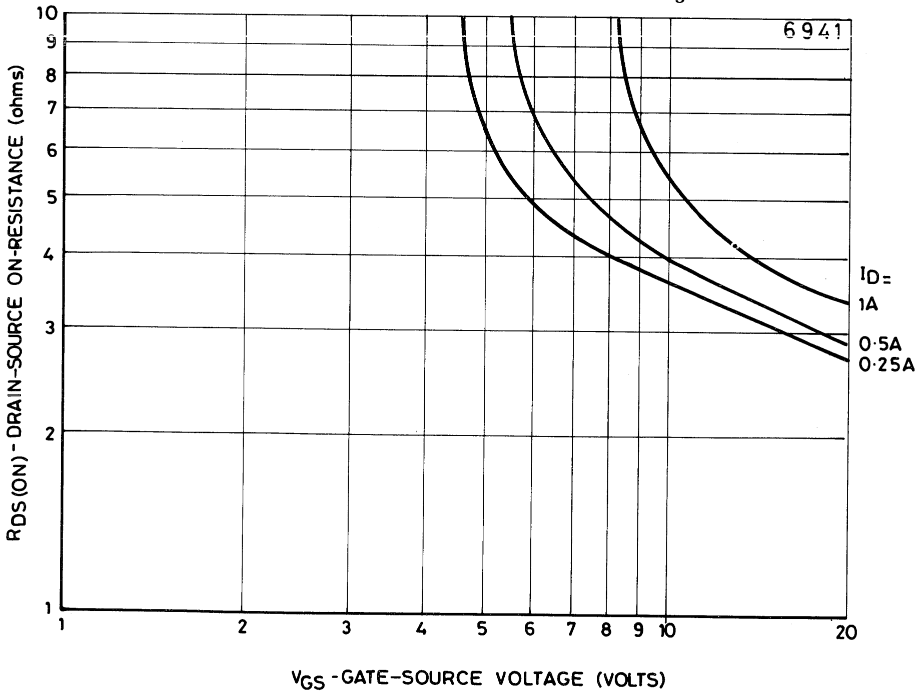


Fig. 9 Variation of $R_{DS(ON)}$ and $V_{GS(th)}$ with Temperature

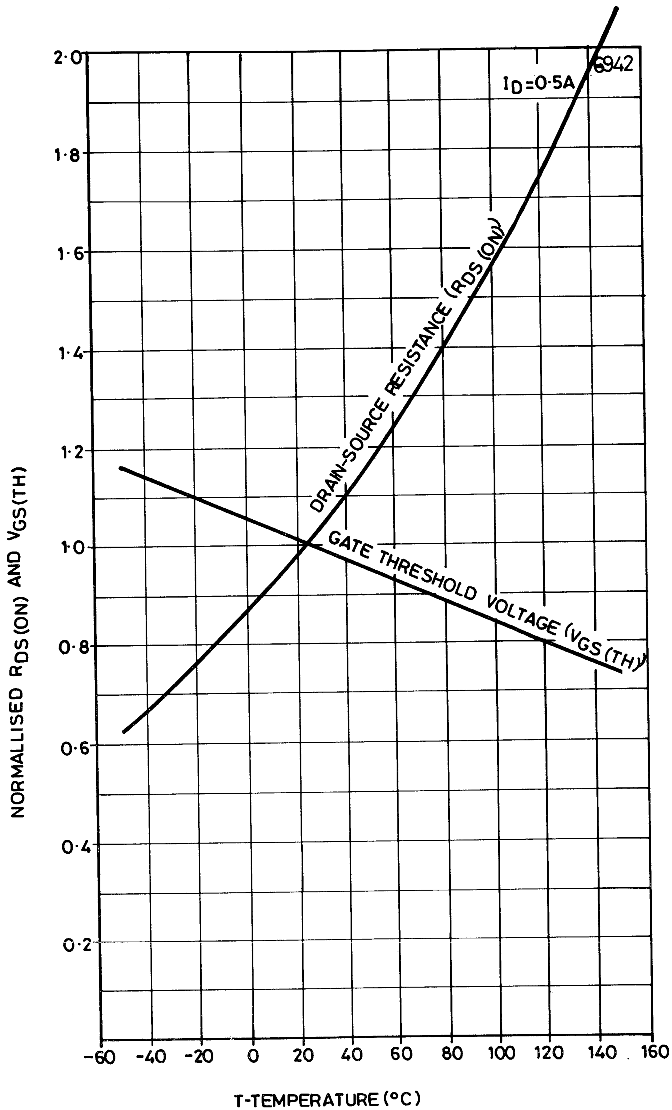
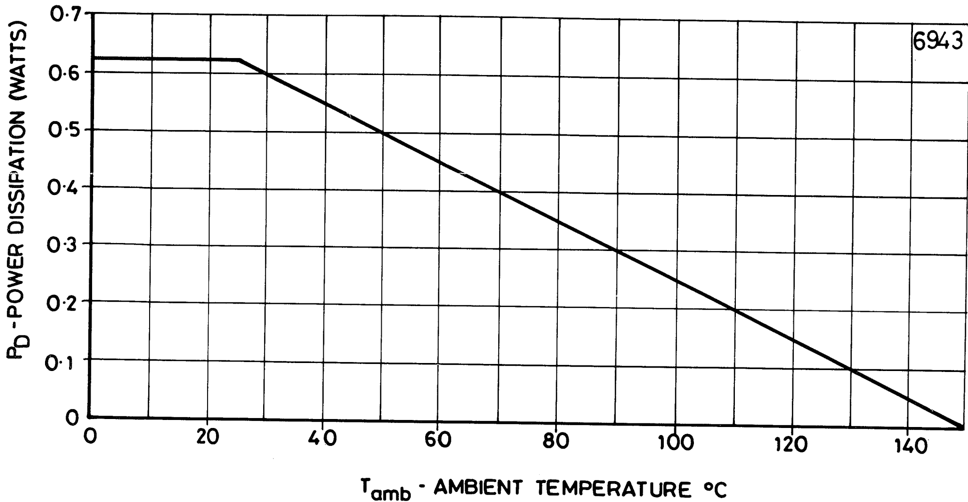


Fig. 10 Power Derating (Ambient)



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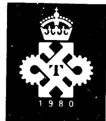
Issue 1, May 1984 4.5M



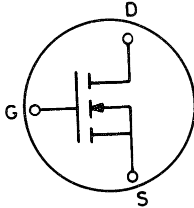
Printed in England CP

ZVN3302B
ZVN3304B
ZVN3306B

FERRANTI semiconductors®

N-Channel Enhancement-Mode Vertical DMOS Power FET

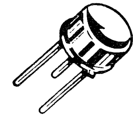
60V: 5 ohm: 0.75A



N-Channel

FEATURES

- Compact Geometry
- Fast Switching Speeds
- No Secondary Breakdown
- Excellent Temperature Stability
- High Input Impedance
- Low Current Drive
- Ease of Paralleling


TO-39 PACKAGE

DESCRIPTION

Compact OVERLAY (CELL) and INTER-DIGITATED geometries are the basis of the new generation of FERRANTI Power MOSFET transistors. These efficient geometries, optimised for low ON-resistance, low capacitances and fast switching speeds, with computer controlled processing combine to achieve greater device ruggedness.

The planar construction, coupled with ion implantation and the self-aligned poly-silicon gate manufacturing process, provides the reliability and stability in performance required in todays designs.

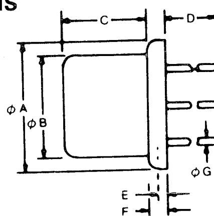
PRODUCT SUMMARY

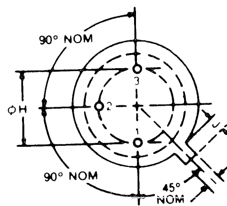
Device Type	BV_{DSS}	$I_{D(CONT)}$	$R_{D(ON)}$
ZVN3302B	20V	0.75A	5Ω
ZVN3304B	40V	0.75A	5Ω
ZVN3306B	60V	0.75A	5Ω

Chip Size 0.030″ × 0.030″

FERRANTI Power MOSFETS will directly interface with MICROPROCESSORS, LOGIC ARRAYS and standard IC LOGIC families including CMOS, TTL, PMOS and NMOS.

PACKAGE DIMENSIONS





PIN OUT	
1	Source
2	Gate
3	Drain & Case

SYMBOL	INCHES		MILLIMETRES	
	MIN	MAX	MIN	MAX
φA	350	370	8 89	9 40
φB	306	335	7 77	8 51
C	240	260	6 10	6 60
D	500		12 70	
E	009	023	229	584
F	018	045	458	1 143
φG	016	021	406	533
φH	190	210	4 83	5 33
I	028	037	711	939
J	026	040	660	1 016

ZVN3302B/3304B/3306B

ABSOLUTE MAXIMUM RATINGS

	Parameters	ZVN3302B	ZVN3304B	ZVN3306B	Units
V_{DS}	Drain-source voltage	20	40	60	V
I_D	Continuous drain current (@ $T_A=25°C$)	0.27			A
I_D	Continuous drain current (@ $T_C=25°C$)	0.75			A
I_{DM}	Pulse drain current	3			A
V_{GS}	Gate-source voltage	±20			V
P_D	Max. power dissipation (@ $T_A=25°C$)	0.625			W
P_D	Max. power dissipation (@ $T_C=25°C$)	5			W
	Operating/Storage Temperature Range	−55 to +150			°C

ELECTRICAL CHARACTERISTICS (at T=25°C unless otherwise stated)

Parameter		Symbol	Min.	Typ.	Max.	Unit	Conditions
Drain source breakdown voltage	ZVN3302B	BV_{DSS}	20	-	-	V	$I_D=1mA$ $V_{GS}=0$
	ZVN3304B		40	-	-		
	ZVN3306B		60	-	-		
Gate-source threshold voltage		$V_{GS(th)}$	0.8	-	2.4	V	$I_D=1mA$, $V_{DS}=V_{GS}$
Gate body leakage		I_{GSS}	-	0.1	20	nA	$V_{GS}=\pm20V$, $V_{DS}=0$
Zero gate voltage Drain current (Note 2)		I_{DSS}	-	-	0.5	μA	V_{DS}=max. rating, $V_{GS}=0$
			-	-	0.05	mA	$V_{DS}=0.8$ × max. rating $V_{GS}=0$ (T=125°C)
On-state drain current*		$I_{D(ON)}$	0.75	1.5	-	A	$V_{DS}=18V$, $V_{GS}=10V$
Static drain-source ON-resistance*		$R_{DS(ON)}$	-	4	5	Ω	$I_D=0.5A$, $V_{GS}=10V$
Forward transconductance* (Note 2)		g_{fs}	0.15	0.18	-	S	$V_{DS}=18V$, $I_D=0.5A$
Input capacitance (Note 2)		C_{iss}	-	31	35	pF	$V_{DS}=18V$ $V_{GS}=0$ f=1MHz
Common source output capacitance (Note 2)		C_{oss}	-	11	25		
Reverse transfer capacitance (Note 2)		C_{rss}	-	3	8		
Turn-ON delay time (Notes 1 & 2)		$t_{d(on)}$	-	3	5	n secs	$V_{DD}=18V$ $I_D=0.5A$
Rise time (Notes 1 & 2)		t_r	-	4	7		
Turn-OFF delay time (Notes 1 & 2)		$t_{d(off)}$	-	4	6		
Fall time (Notes 1 & 2)		t_f	-	5	8		

*Measured under pulsed conditions. Width=300μs. Duty cycle ⩽2%.

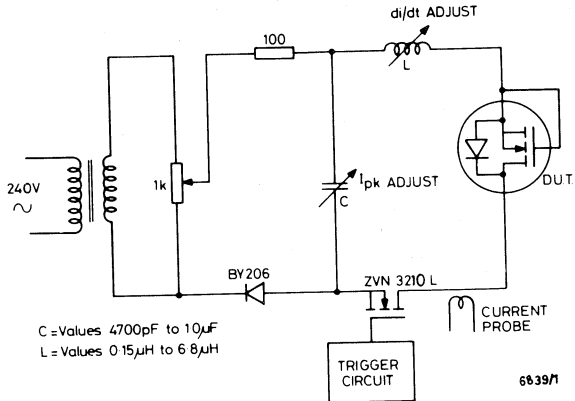
Note 1 Switching times measured with 50 ohm source impedance and <5ns rise time on a pulse generator.

Note 2 Sample test.

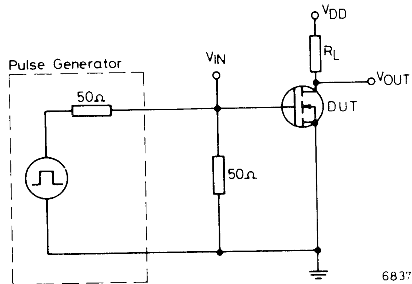
DRAIN-SOURCE DIODE CHARACTERISTICS

Parameter	Symbol	Typ.	Unit	Conditions
Forward ON voltage*	V_{SD}	1.06	V	$V_{GS}=0$, $I_S=750mA$
Reverse recovery time	t_{rr}	155	n secs	$V_{GS}=0$, $I_F=750mA$, $I_R=100mA$

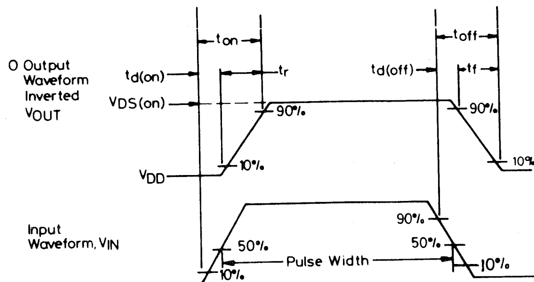
Reverse Recovery Test Circuit



Circuit for Measuring Switching Times



Switching Waveforms



Note:
Power MOSFET switching times are essentially independent of operating temperature

Fig. 1 Saturation Characteristics

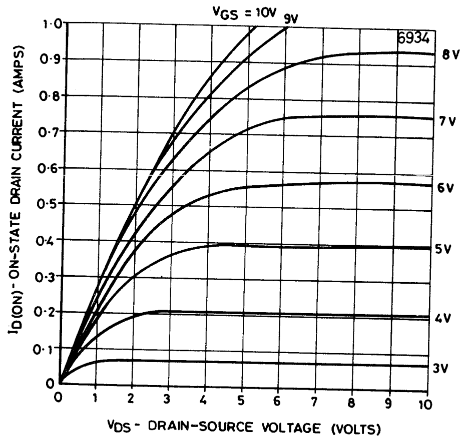


Fig. 2 Voltage Saturation Characteristics

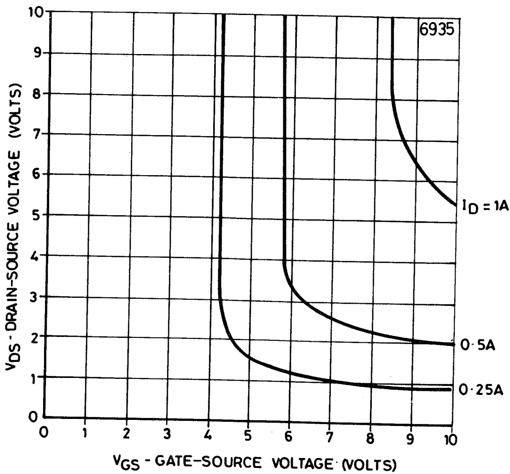


Fig. 3 Transfer Characteristics

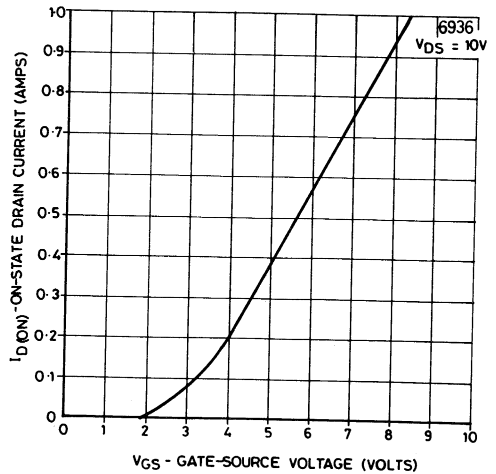


Fig. 4 Capacitance vs Drain-Source Voltage

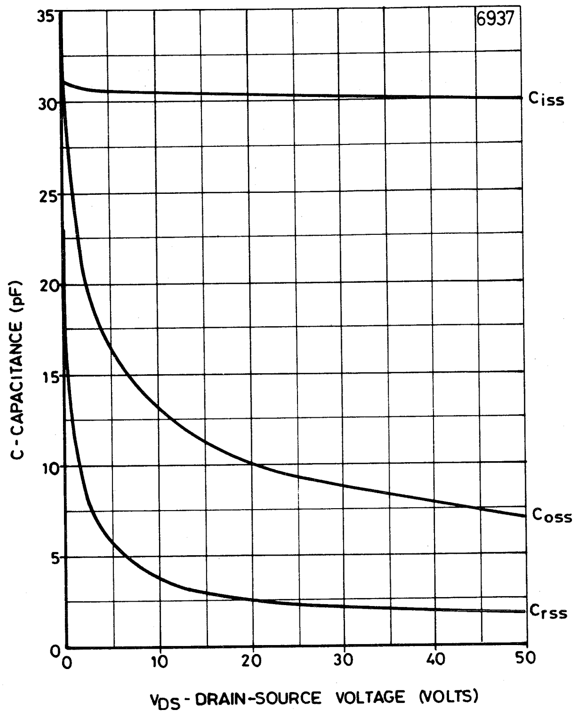


Fig. 5 Transconductance vs Drain-Current

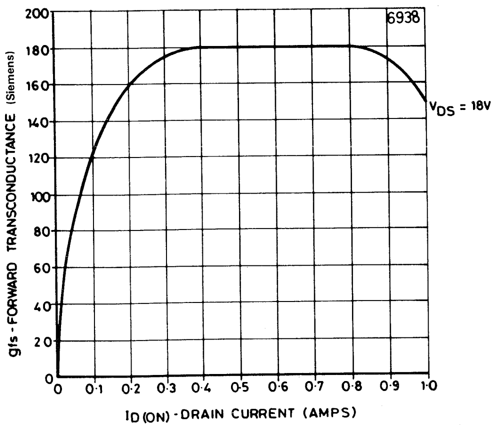


Fig. 6 Transconductance vs Gate-Source Voltage

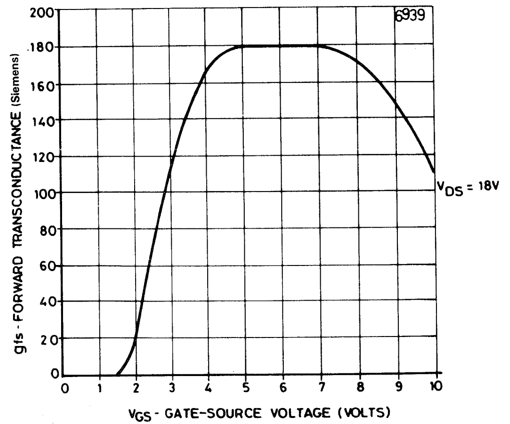


Fig. 7 Gate Charge vs Gate-Source Voltage

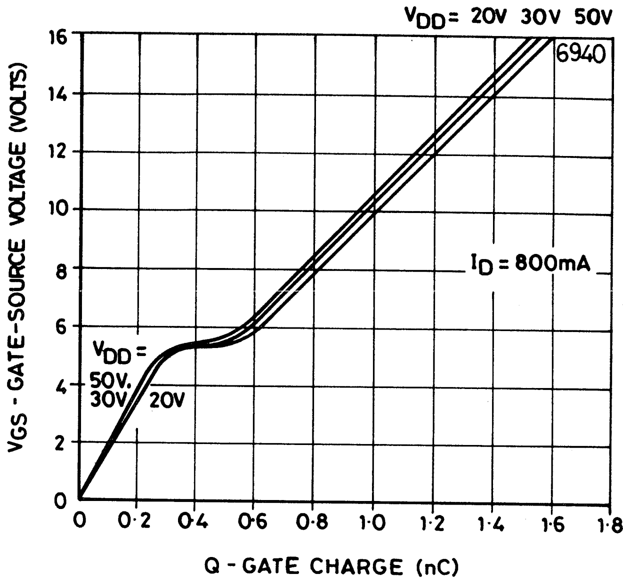


Fig. 8 ON-Resistance vs Gate-Source Voltage

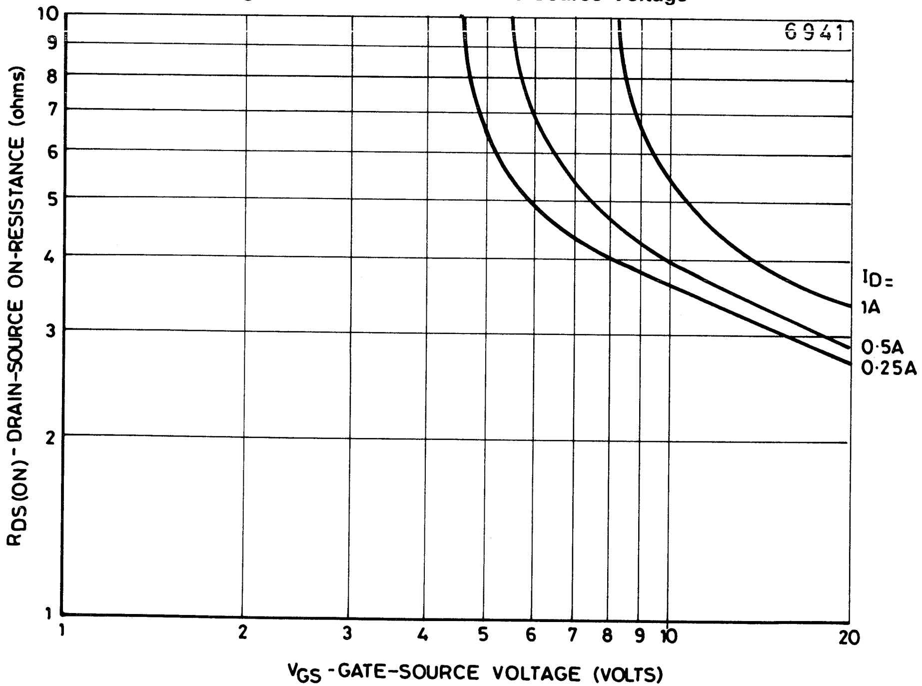
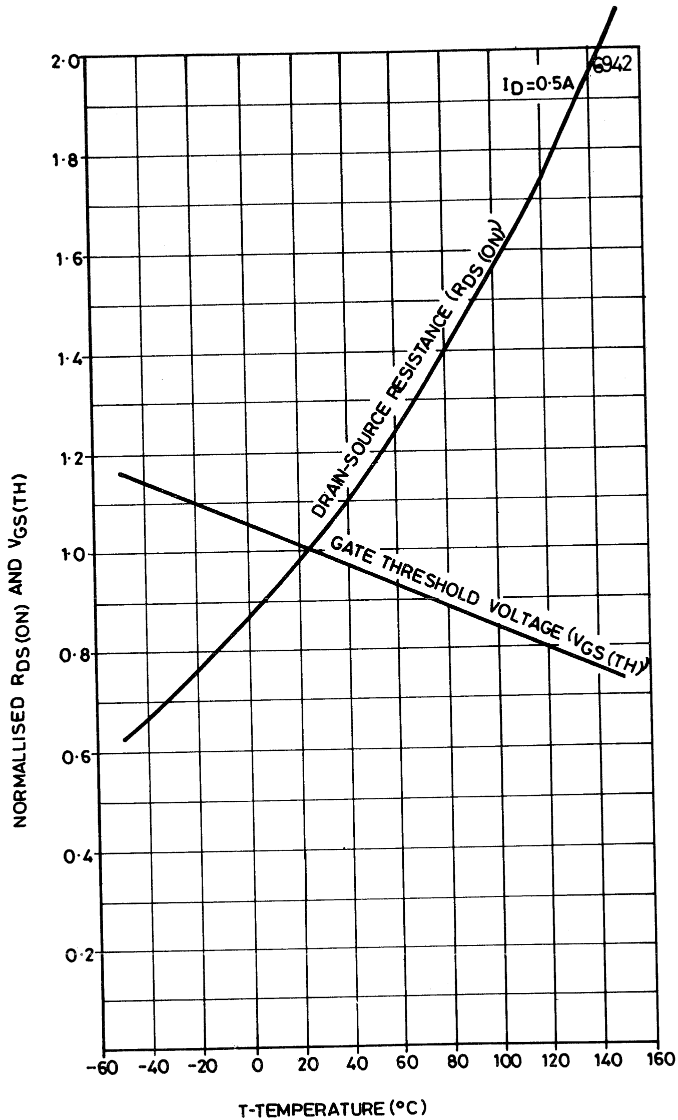


Fig. 9 Variation of $R_{DS(ON)}$ and $V_{GS(th)}$ with Temperature



ZVN3302B/3304B/3306B

Fig. 10 Power Derating (Ambient)

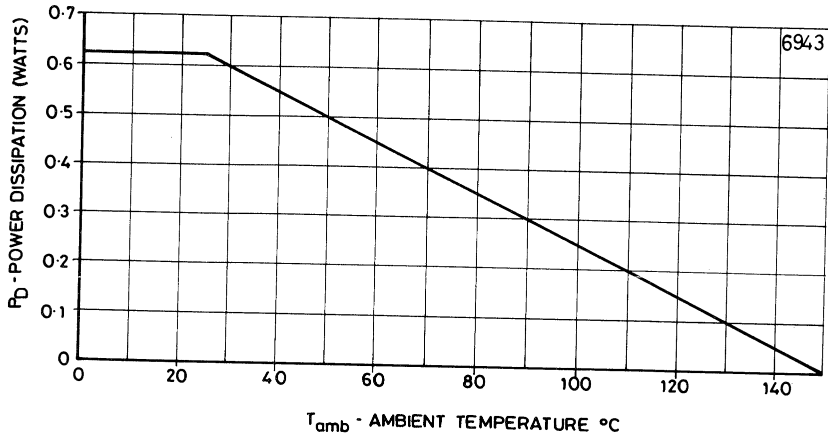
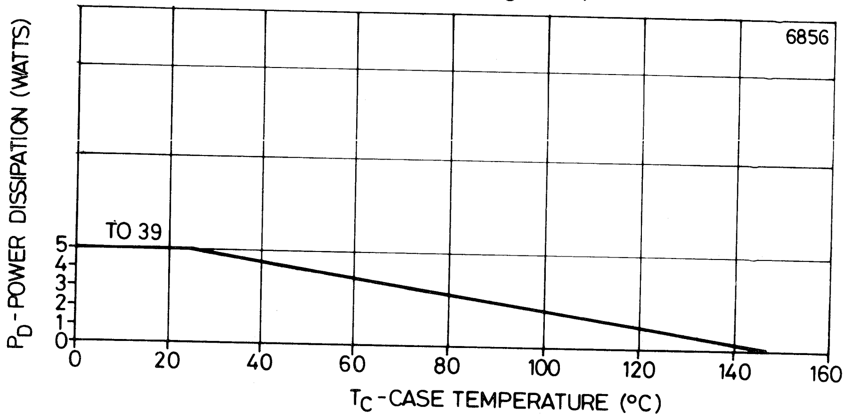


Fig. 11 Power Derating (Case)



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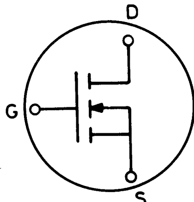
Issue 1, August 1984 5.1M

FERRANTI semiconductors ®

N-Channel Enhancement-Mode Vertical DMOS Power FET

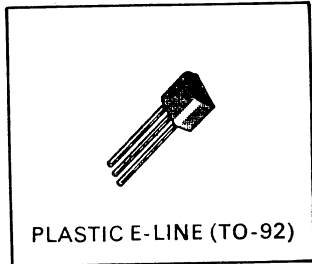
100V: 10 ohm: 0.2A



N-Channel

FEATURES

- Compact Geometry
- Fast Switching Speeds
- No Secondary Breakdown
- Excellent Temperature Stability
- High Input Impedance
- Low Current Drive



PLASTIC E-LINE (TO-92)

DESCRIPTION

Compact OVERLAY (CELL) and INTER-DIGITATED geometries are the basis of the new generation of FERRANTI Power MOSFET transistors. These efficient geometries, optimised for low ON-resistance, low capacitances and fast switching speeds, with computer controlled processing combine to achieve greater device ruggedness.

The planar construction, coupled with ion implantation and the self-aligned poly-silicon gate manufacturing process, provides the reliability and stability in performance required in todays designs.

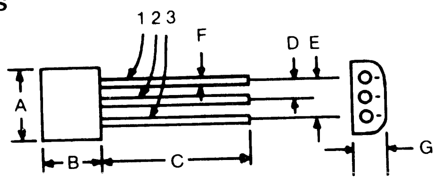
PRODUCT SUMMARY

Device Type	BV_{DSS}	$I_{D(CONT)}$	$R_{D(ON)}$
ZVN1306A	60V	0.2A	10Ω
ZVN1308A	80V	0.2A	10Ω
ZVN3310A	100V	0.2A	10Ω

Chip Size 0.030″ × 0.030″

FERRANTI Power MOSFETS will directly interface with MICROPROCESSORS, LOGIC ARRAYS and standard IC LOGIC families including CMOS; TTL, PMOS and NMOS.

PACKAGE DIMENSIONS



PIN OUT	
1	Drain
2	Gate
3	Source

Also available with various lead bends and on Tape and Reel.

SYMBOL	INCHES		MILLIMETRES	
	MIN	MAX	MIN	MAX
A	.172	.188	4.37	4.77
B	.142	.158	3.61	4.01
C	.475	.525	12.06	13.34
D	.05		1.27	
E	.10		2.54	
F	.016	.019	.406	.495
G	.085	.095	2.16	2.42

ZVN1306A/1308A/3310A

ABSOLUTE MAXIMUM RATINGS

	Parameters	ZVN1306A	ZVN1308A	ZVN3310A	Units
V_{DS}	Drain-source voltage	60	80	100	V
I_D	Continuous drain current (@ $T_A = 25°C$)	0.20			A
I_D	Continuous drain current (@ $T_C = 25°C$)	-			A
I_{DM}	Pulse drain current	2			A
V_{GS}	Gate-source voltage	± 20			V
P_D	Max. Power Dissipation (@ $T_A = 25°C$)	0.625			W
P_D	Max. Power Dissipation (@ $T_C = 25°C$)	-			W
	Operating/Storage Temperature Range	-55 to $+150$			°C

ELECTRICAL CHARACTERISTICS (at T = 25°C unless otherwise stated)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Drain source breakdown voltage ZVN1306A	BV_{DSS}	60	-	-	V	$I_D = 1mA$, $V_{GS} = 0$
Drain source breakdown voltage ZVN1308A		80	-	-		
Drain source breakdown voltage ZVN3310A		100	-	-		
Gate-source threshold voltage	$V_{GS(th)}$	0.8	-	2.4	V	$I_D = 1mA$, $V_{DS} = V_{GS}$
Gate body leakage	I_{GSS}	-	0.1	20	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0$
Zero gate voltage Drain current (Note 2)	I_{DSS}	-		1	μA	V_{DS} = max. rating, $V_{GS} = 0$
		-	-	0.05	mA	$V_{DS} = 0.8 \times$ max. rating $V_{GS} = 0$ ($T = 125°C$)
On-state drain current*	$I_{D(ON)}$	0.5	1.1	-	A	$V_{DS} = 25V$, $V_{GS} = 10V$
Static drain-source ON-resistance*	$R_{DS(ON)}$	-	5	10	Ω	$I_D = 0.5A$, $V_{GS} = 10V$
Forward transconductance* (Note 2)	g_{fs}	0.10	0.16	-	S	$V_{DS} = 25V$, $I_D = 0.5A$
Input capacitance (Note 2)	C_{iss}	-	25	40	pF	$V_{DS} = 25V$, $V_{GS} = 0$, $f = 1MHz$
Common source output capacitance (Note 2)	C_{oss}	-	8	15		
Reverse transfer capacitance (Note 2)	C_{rss}	-	3	5		
Turn-ON delay time (Notes 1 & 2)	$t_{d(on)}$	-	3	5	n secs	$V_{DD} = 25V$, $I_D = 0.5A$
Rise time (Notes 1 & 2)	t_r	-	5	7		
Turn-OFF delay time (Notes 1 & 2)	$t_{d(off)}$	-	4	6		
Fall time (Notes 1 & 2)	t_f	-	5	7		

* Measured under pulsed conditions. Width = 300μs. Duty cycle ≤ 2%.

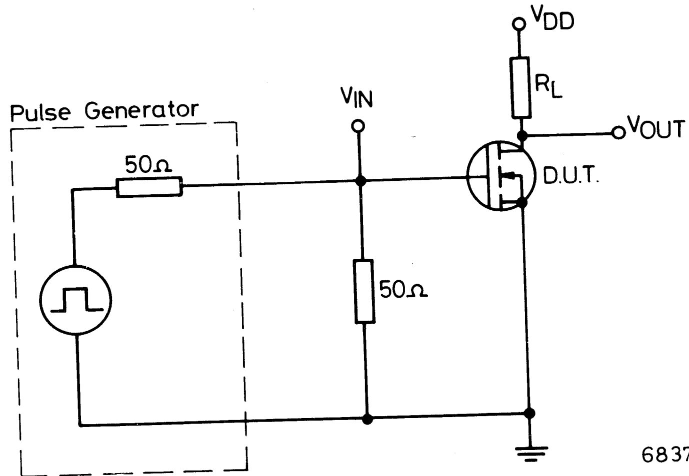
Note 1 Switching times measured with 50 ohm source impedance and <5ns rise time on a pulse generator.

Note 2 Sample test.

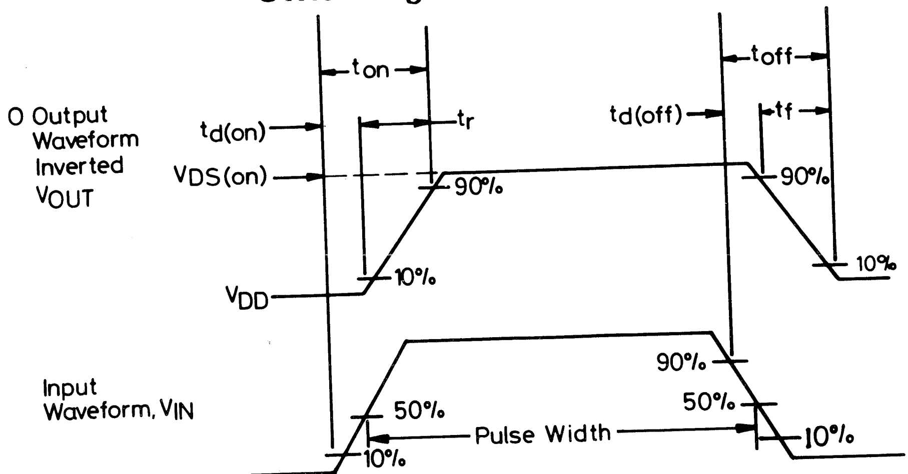
DRAIN-SOURCE DIODE CHARACTERISTICS

Parameter	Symbol	Typ.	Unit	Conditions
Forward ON voltage*	V_{SD}	0.82	V	$V_{GS}=0$, $I_S=0.2A$

Circuit for Measuring Switching Times



Switching Waveforms

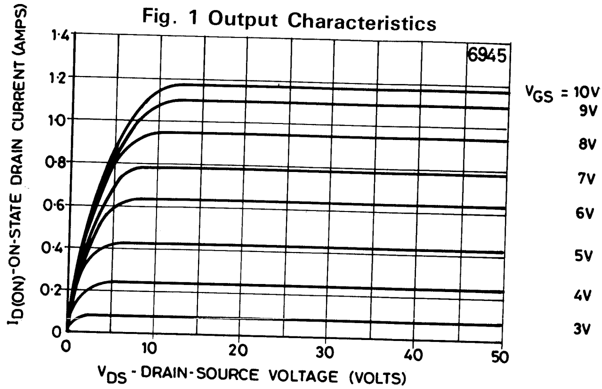


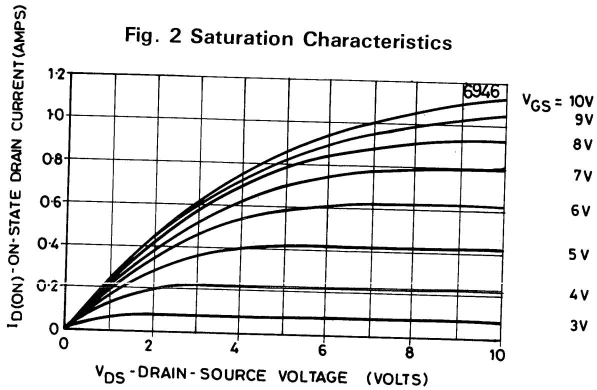
Input voltage amplitude 10 Volts peak

6838/1

Note:
Power MOSFET switching
times are essentially independent
of operating temperature

ZVN1306A/1308A/3310A





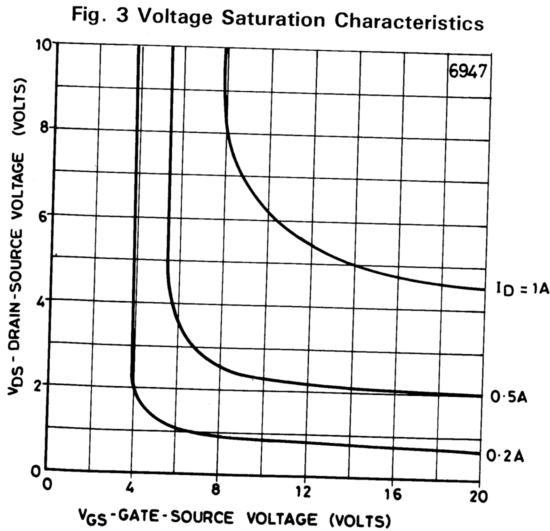


Fig. 4 Transfer Characteristics

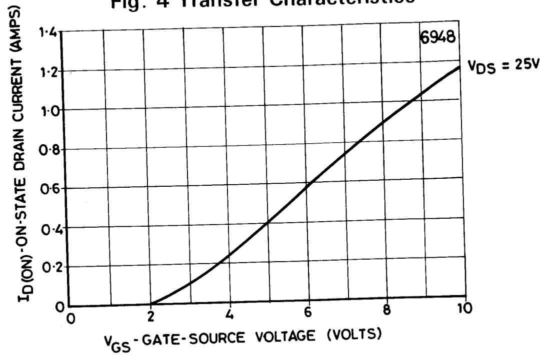


Fig. 5 Capacitance vs Drain-Source Voltage

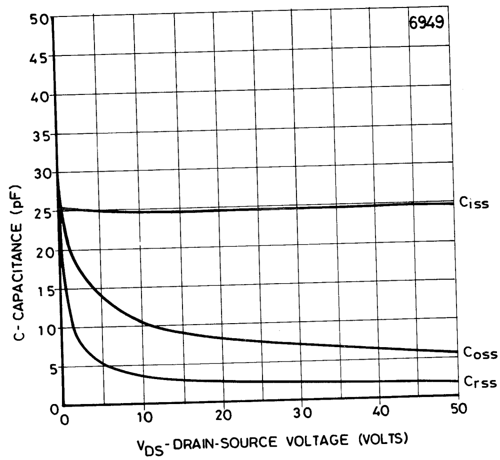


Fig. 6 Transconductance vs Drain-Current

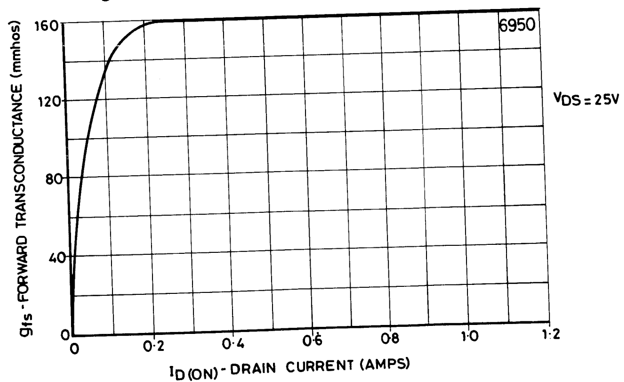


Fig. 7 Transconductance vs Gate-Source Voltage

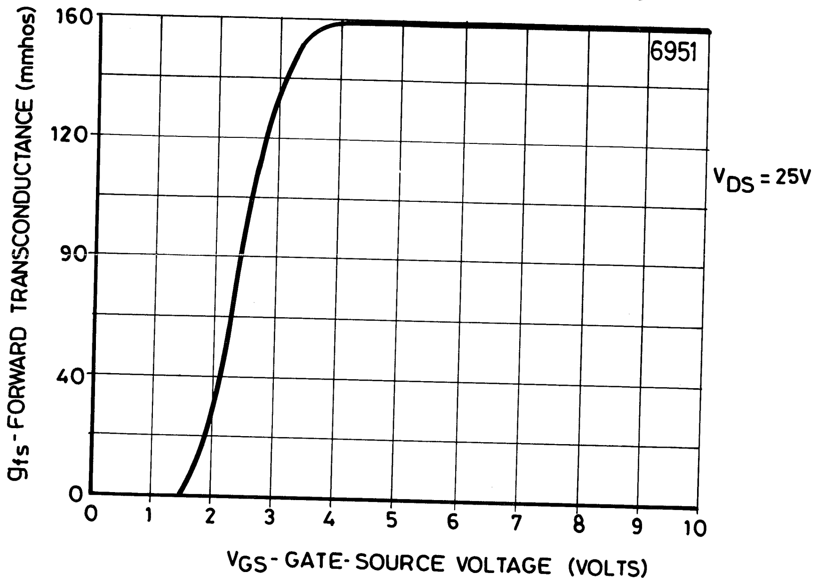


Fig. 8 Gate Charge vs Gate-Source Voltage

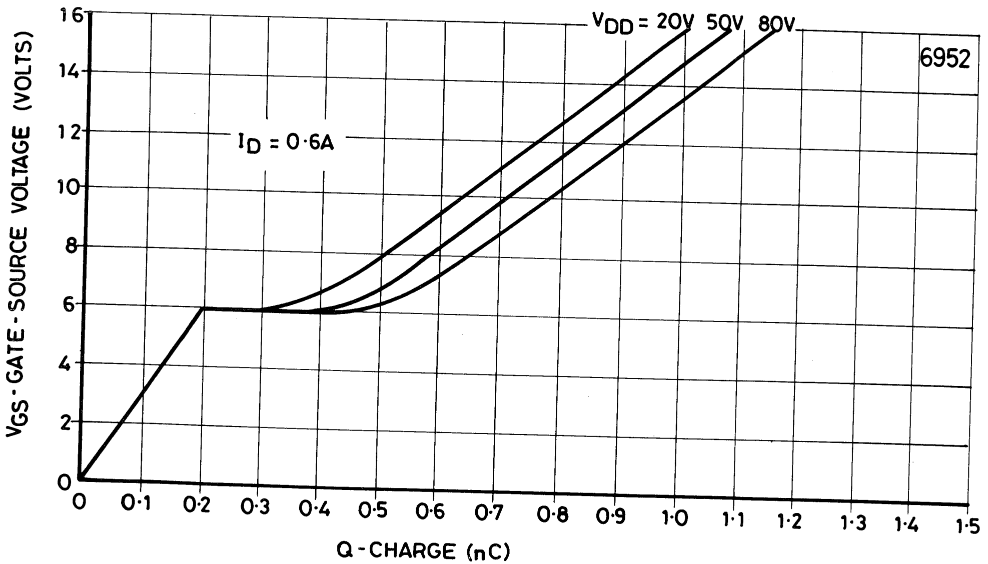


Fig. 9 ON-Resistance vs Gate-Source Voltage

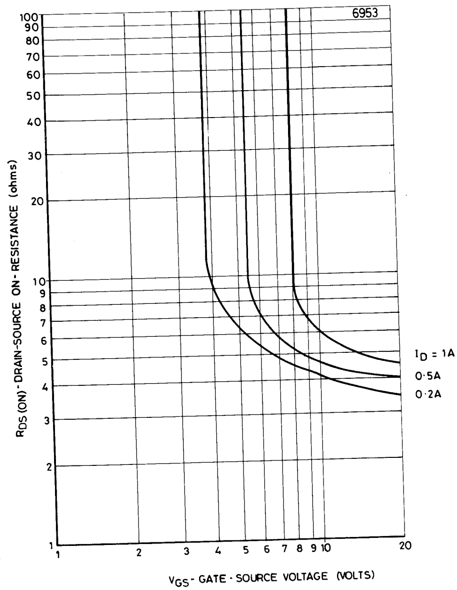


Fig. 10 Variation of $R_{DS(ON)}$ and $V_{GS(th)}$ with Temperature

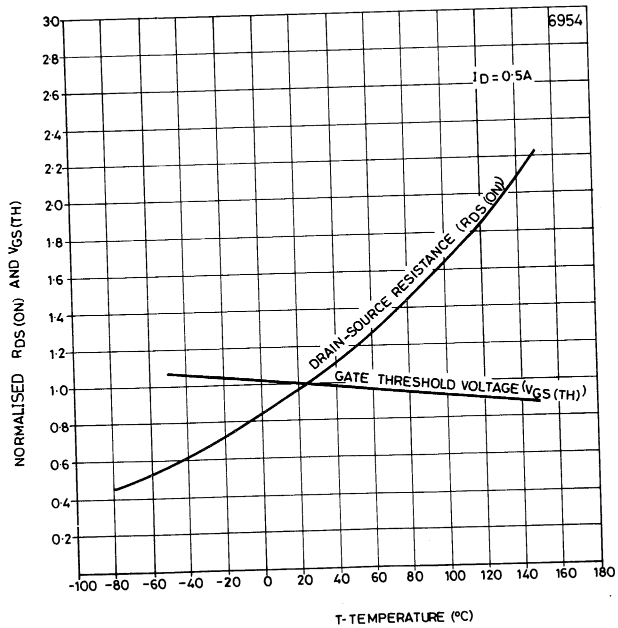
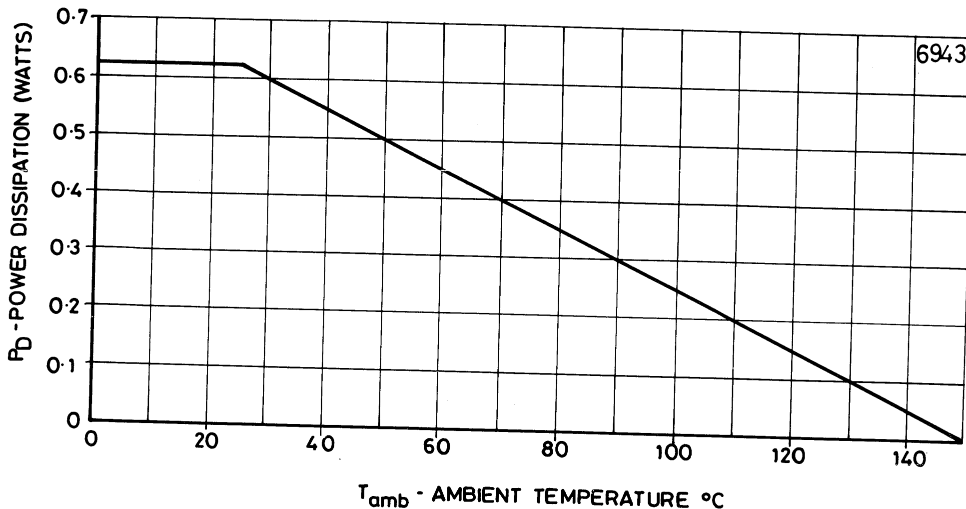


Fig. 11 Power Derating (Ambient)



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Issue 1, May 1984 4.5M

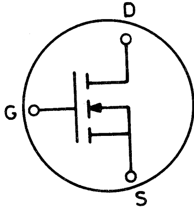
Printed in England CP

ZVN1306B
ZVN1308B
ZVN3310B

FERRANTI semiconductors ®

N-Channel Enhancement-Mode Vertical DMOS Power FET

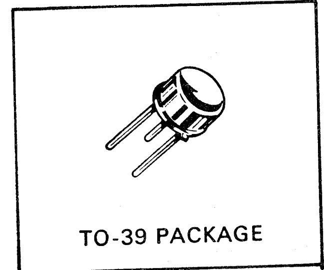
100V: 10 ohm: 0.5A



N-Channel

FEATURES

- Compact Geometry
- Fast Switching Speeds
- No Secondary Breakdown
- Excellent Temperature Stability
- High Input Impedance
- Low Current Drive



TO-39 PACKAGE

DESCRIPTION

Compact OVERLAY (CELL) and INTER-DIGITATED geometries are the basis of the new generation of FERRANTI Power MOSFET transistors. These efficient geometries, optimised for low ON-resistance, low capacitances and fast switching speeds, with computer controlled processing combine to achieve greater device ruggedness.

The planar construction, coupled with ion implantation and the self-aligned poly-silicon gate manufacturing process, provides the reliability and stability in performance required in todays designs.

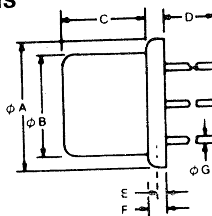
PRODUCT SUMMARY

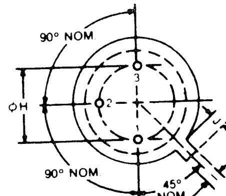
Device Type	BV_{DSS}	$I_{D(CONT)}$	$R_{D(ON)}$
ZVN1306B	60V	0.5A	10Ω
ZVN1308B	80V	0.5A	10Ω
ZVN3310B	100V	0.5A	10Ω

Chip Size 0.030″ × 0.030″

FERRANTI Power MOSFETS will directly interface with MICROPROCESSORS, LOGIC ARRAYS and standard IC LOGIC families including CMOS, TTL, PMOS and NMOS.

PACKAGE DIMENSIONS





PIN OUT	
1	Source
2	Gate
3	Drain & Case

SYMBOL	INCHES		MILLIMETRES	
	MIN	MAX	MIN	MAX
ϕA	.350	370	8.89	9.40
ϕB	.306	335	7.77	8.51
C	.240	.260	6.10	6 60
D	.500		12.70	
E	.009	.023	.229	584
F	.018	.045	458	1 143
ϕG	.016	.021	.406	533
ϕH	.190	.210	4.83	5 33
I	.028	.037	711	.939
J	.026	.040	660	1 016

ZVN1306B/1308B/3310B

ABSOLUTE MAXIMUM RATINGS

	Parameters	ZVN1306B	ZVN1308B	ZVN3310B	Units
V_{DS}	Drain-source voltage	60	80	100	V
I_D	Continuous drain current (@ $T_A=25°C$)	0.20			A
I_D	Continuous drain current (@ $T_C=25°C$)	0.5			A
I_{DM}	Pulse drain current	2			A
V_{GS}	Gate-source voltage	±20			V
P_D	Max. Power Dissipation (@ $T_A=25°C$)	0.625			W
P_D	Max. Power Dissipation (@ $T_C=25°C$)	5			W
	Operating/Storage Temperature Range	−55 to +150			°C

ELECTRICAL CHARACTERISTICS (at T=25°C unless otherwise stated)

Parameter		Symbol	Min.	Typ.	Max.	Unit	Conditions
Drain source breakdown voltage	ZVN1306B	BV_{DSS}	60	-	-	V	$I_D=1mA$, $V_{GS}=0$
	ZVN1308B		80	-	-		
	ZVN3310B		100	-	-		
Gate-source threshold voltage		$V_{GS(th)}$	0.8	-	2.4	V	$I_D=1mA$, $V_{DS}=V_{GS}$
Gate body leakage		I_{GSS}	-	0.1	20	nA	$V_{GS}=\pm20V$, $V_{DS}=0$
Zero gate voltage Drain current (Note 2)		I_{DSS}	-	-	1	µA	V_{DS} = max. rating, $V_{GS}=0$
			-	-	0.05	mA	$V_{DS}=0.8 \times$ max. rating $V_{GS}=0$ (T=125°C)
On-state drain current*		$I_{D(ON)}$	0.5	1.1	-	A	$V_{DS}=25V$, $V_{GS}=10V$
Static drain-source ON-resistance*		$R_{DS(ON)}$	-	5	10	Ω	$I_D=0.5A$, $V_{GS}=10V$
Forward transconductance* (Note 2)		g_{fs}	0.10	0.16	-	S	$V_{DS}=25V$, $I_D=0.5A$
Input capacitance (Note 2)		C_{iss}	-	25	40	pF	$V_{DS}=25V$, $V_{GS}=0$, f=1MHz
Common source output capacitance (Note 2)		C_{oss}	-	8	15		
Reverse transfer capacitance (Note 2)		C_{rss}	-	3	5		
Turn-ON delay time (Notes 1 & 2)		$t_{d(on)}$	-	3	5	n secs	$V_{DD}=25V$, $I_D=0.5A$
Rise time (Notes 1 & 2)		t_r	-	5	7		
Turn-OFF delay time (Notes 1 & 2)		$t_{d(off)}$	-	4	6		
Fall time (Notes 1 & 2)		t_f	-	5	7		

*Measured under pulsed conditions. Width = 300µs. Duty cycle ⩽ 2%.

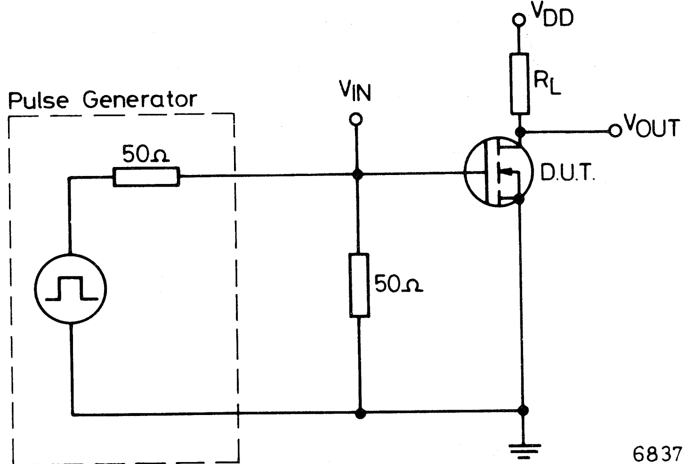
Note 1 Switching times measured with 50 ohm source impedance and <5ns rise time on a pulse generator.

Note 2 Sample test.

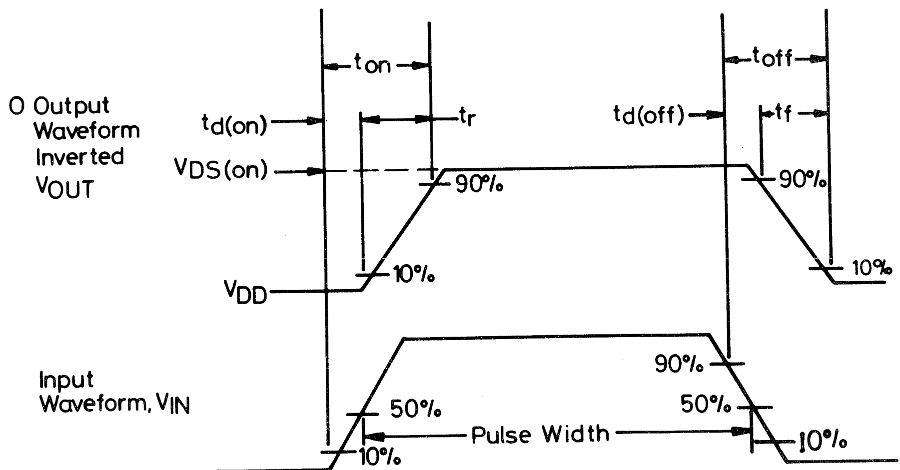
DRAIN-SOURCE DIODE CHARACTERISTICS

Parameter	Symbol	Typ.	Unit	Conditions
Forward ON voltage*	V_{SD}	0.92	V	$V_{GS}=0$, $I_S=0.5A$

Circuit for Measuring Switching Times



Switching Waveforms



Input voltage amplitude 10 Volts peak

6838/1

Note:
Power MOSFET switching times are essentially independent of operating temperature

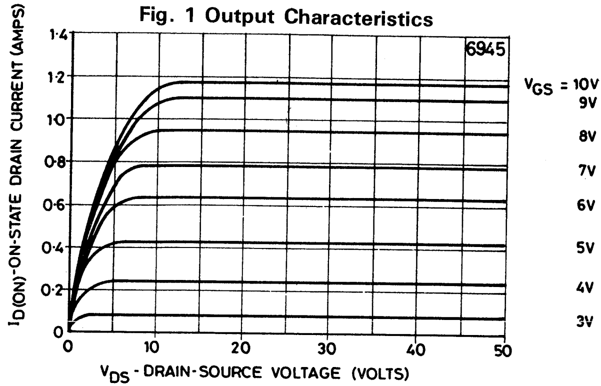


Fig. 1 Output Characteristics
6945
$I_{D(ON)}$-ON-STATE DRAIN CURRENT (AMPS)
1·4
1·2
1·0
0·8
0·6
0·4
0·2
0
10
20
30
40
50
V_{GS} = 10V
9V
8V
7V
6V
5V
4V
3V
V_{DS} - DRAIN-SOURCE VOLTAGE (VOLTS)

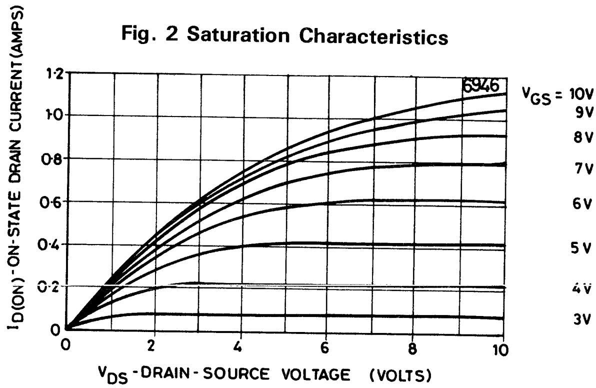


Fig. 2 Saturation Characteristics
6946
$I_{D(ON)}$-ON-STATE DRAIN CURRENT (AMPS)
1·2
1·0
0·8
0·6
0·4
0·2
0
2
4
6
8
10
V_{GS} = 10V
9V
8V
7V
6V
5V
4V
3V
V_{DS} - DRAIN - SOURCE VOLTAGE (VOLTS)

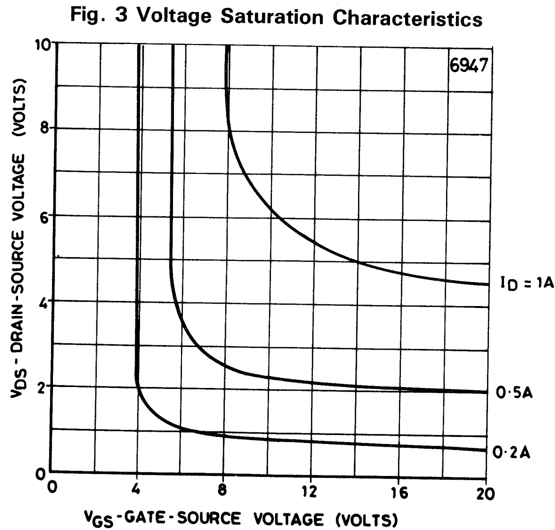


Fig. 3 Voltage Saturation Characteristics
6947
V_{DS} - DRAIN-SOURCE VOLTAGE (VOLTS)
10
8
6
4
2
0
4
8
12
16
20
I_D = 1A
0·5A
0·2A
V_{GS} - GATE - SOURCE VOLTAGE (VOLTS)

Fig. 4 Transfer Characteristics

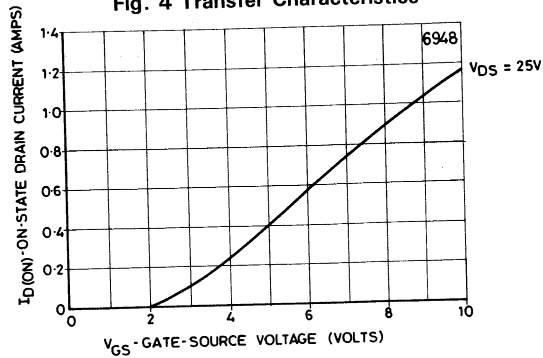


Fig. 5 Capacitance vs Drain-Source Voltage

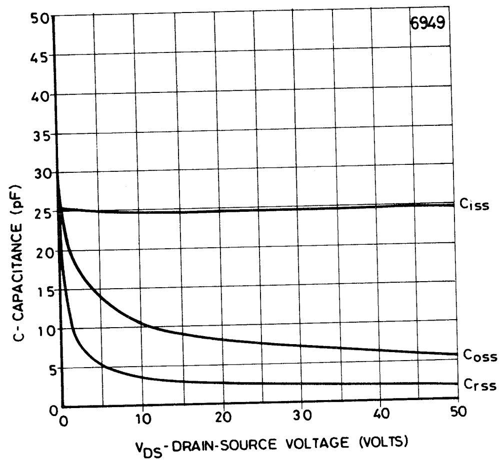


Fig. 6 Transconductance vs Drain-Current

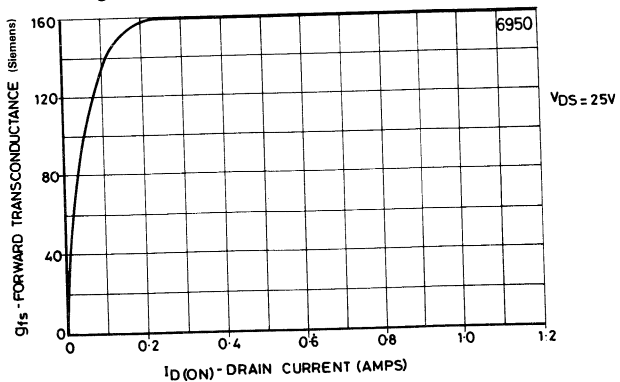


Fig. 7 Transconductance vs Gate-Source Voltage

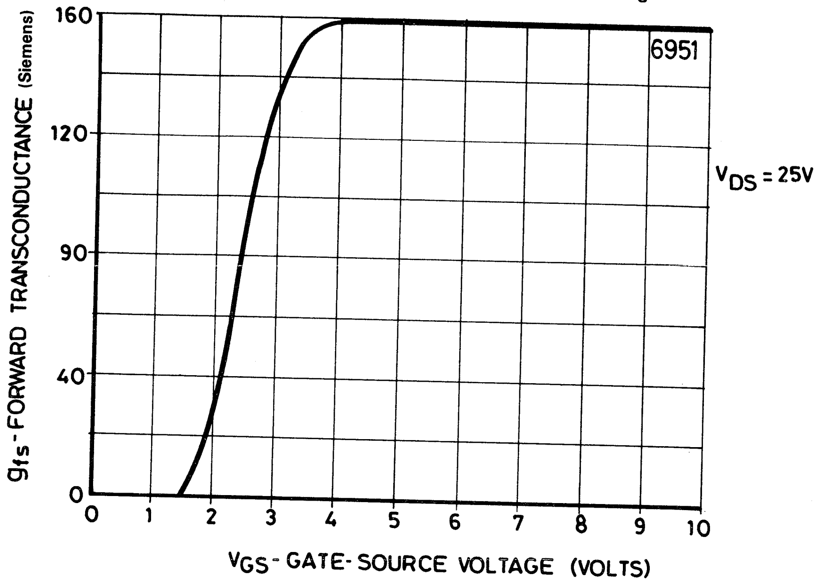


Fig. 8 Gate Charge vs Gate-Source Voltage

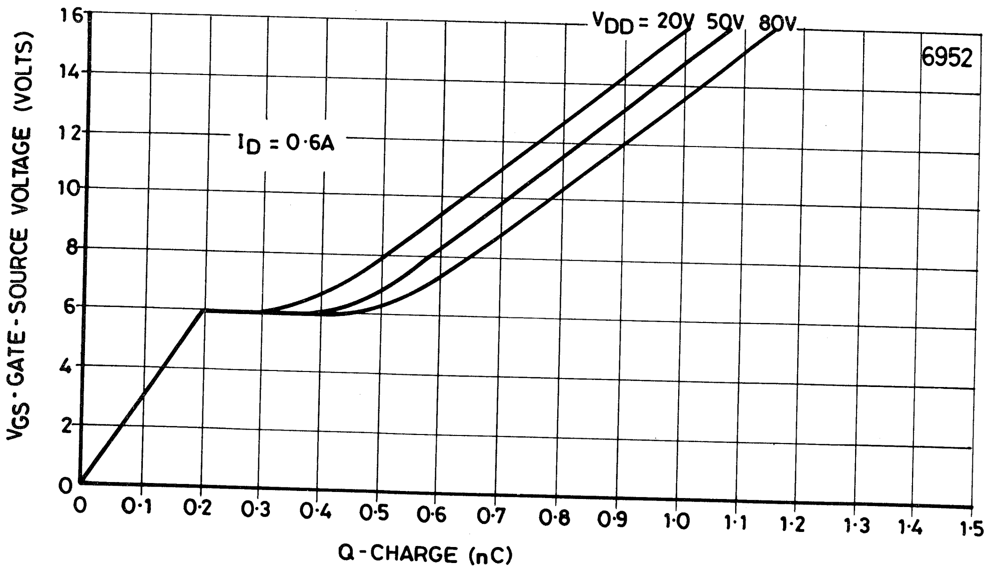


Fig. 9 ON-Resistance vs Gate-Source Voltage

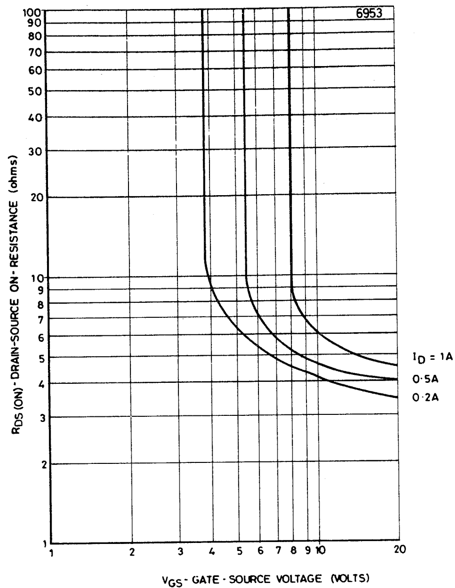


Fig. 10 Variation of $R_{DS(ON)}$ and $V_{GS(th)}$ with Temperature

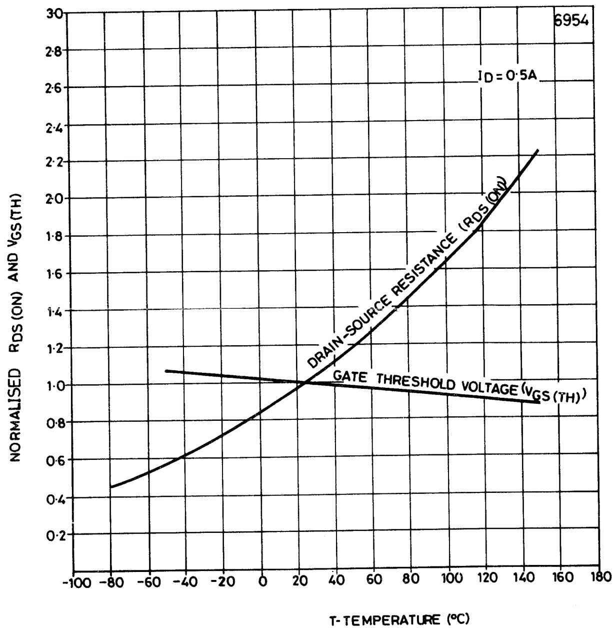


Fig. 11 Power Derating (Ambient)

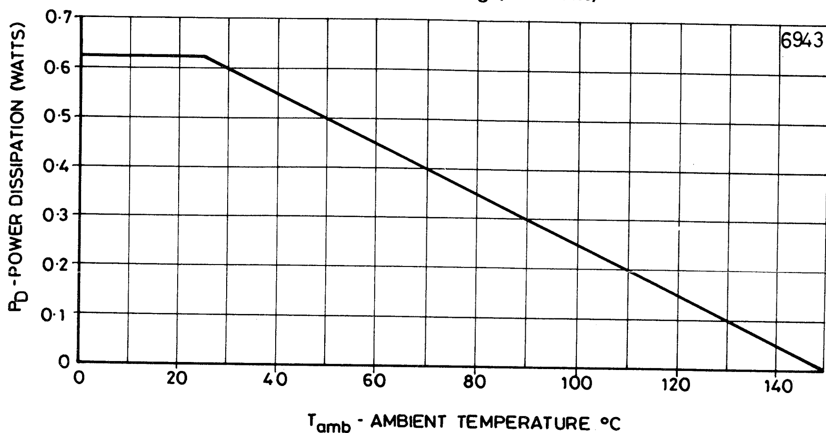
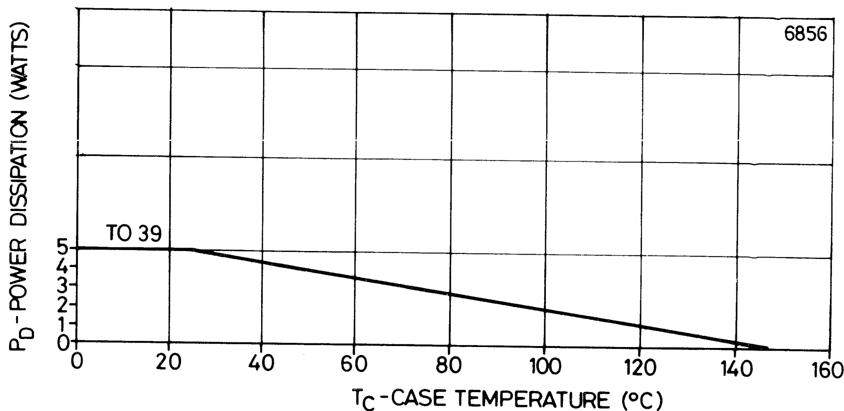


Fig. 12 Power Derating (Case)



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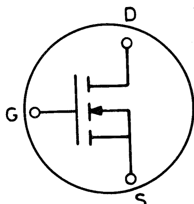
Issue 1, August 1984 5.1M

ZVN3315A
ZVN1320A

FERRANTI semiconductors ®

N-Channel Enhancement-Mode Vertical DMOS Power FET

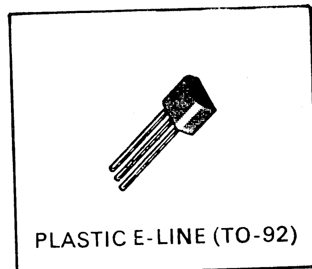
200V: 40 ohm: 0.1A



N-Channel

FEATURES

- Compact Geometry
- Fast Switching Speeds
- No Secondary Breakdown
- Excellent Temperature Stability
- High Input Impedance
- Low Current Drive
- Ease of Paralleling



PLASTIC E-LINE (TO-92)

DESCRIPTION

Compact OVERLAY (CELL) and INTER-DIGITATED geometries are the basis of the new generation of FERRANTI Power MOSFET transistors. These efficient geometries, optimised for low ON-resistance, low capacitances and fast switching speeds, with computer controlled processing combine to achieve greater device ruggedness.

The planar construction, coupled with ion implantation and the self-aligned poly-silicon gate manufacturing process, provides the reliability and stability in performance required in todays designs.

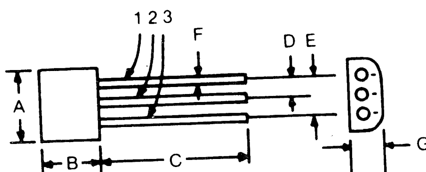
PRODUCT SUMMARY

Device Type	BV_{DSS}	$I_{D(CONT)}$	$R_{D(ON)}$
ZVN3315A	150V	0.1A	40Ω
ZVN1320A	200V	0.1A	40Ω

Chip Size 0.030″ × 0.030″

FERRANTI Power MOSFETS will directly interface with MICROPROCESSORS, LOGIC ARRAYS and standard IC LOGIC families including CMOS, TTL, PMOS and NMOS.

PACKAGE DIMENSIONS



PIN OUT	
1	Drain
2	Gate
3	Source

SYMBOL	INCHES		MILLIMETRES	
	MIN	MAX	MIN	MAX
A	.172	.188	4.37	4.77
B	.142	.158	3.61	4.01
C	.475	.525	12.06	13.34
D	.05		1.27	
E	.10		2.54	
F	.016	.019	.406	.495
G	.085	.095	2.16	2.42

Also available with various lead bends and on Tape and Reel.

ZVN3315A/1320A

ABSOLUTE MAXIMUM RATINGS

Parameters		ZVN3315A	ZVN1320A	Units
V_{DS}	Drain-source voltage	150	200	V
I_D	Continuous drain current (@ $T_A = 25°C$)	0.1		A
I_D	Continuous drain current (@ $T_C = 25°C$)	-		A
I_{DM}	Pulse drain current	1		A
V_{GS}	Gate-source voltage	±20		V
P_D	Max. power dissipation (@ $T_A = 25°C$)	0.625		W
P_D	Max. power dissipation (@ $T_C = 25°C$)	-		W
	Operating/Storage Temperature Range	−55 to +150		°C

ELECTRICAL CHARACTERISTICS (at T = 25°C unless otherwise stated)

Parameter		Symbol	Min.	Typ.	Max.	Unit	Conditions
Drain source breakdown voltage	ZVN3315A	BV_{DSS}	150	-	-	V	$I_D = 1mA$ $V_{GS} = 0$
	ZVN1320A		200	-	-		
Gate-source threshold voltage		$V_{GS(th)}$	1	-	3	V	$I_D = 1mA$, $V_{DS} = V_{GS}$
Gate body leakage		I_{GSS}	-	0.1	100	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0$
Zero gate voltage Drain current (Note 2)		I_{DSS}	-	-	10	μA	V_{DS} = max. rating, $V_{GS} = 0$
			-	-	0.05	mA	$V_{DS} = 0.8 \times$ max. rating $V_{GS} = 0$ (T = 125°C)
On-state drain current*		$I_{D(ON)}$	0.25	0.37	-	A	$V_{DS} = 25V$, $V_{GS} = 10V$
Static drain-source ON-resistance*		$R_{DS(ON)}$	-	22	40	Ω	$I_D = 0.1A$, $V_{GS} = 10V$
Forward transconductance* (Note 2)		g_{fs}	0.075	0.11	-	S	$V_{DS} = 25V$, $I_D = 0.1A$
Input capacitance (Note 2)		C_{iss}	-	28	45	pF	$V_{DS} = 25V$ $V_{GS} = 0$ f = 1MHz
Common source output capacitance (Note 2)		C_{oss}	-	14	18	pF	
Reverse transfer capacitance (Note 2)		C_{rss}	-	2	5	pF	
Turn-ON delay time (Notes 1 & 2)		$t_{d(on)}$	-	3	5	n secs	$V_{DD} = 25V$ $I_D = 0.1A$
Rise time (Notes 1 & 2)		t_r	-	5	7	n secs	
Turn-OFF delay time (Notes 1 & 2)		$t_{d(off)}$	-	4	6	n secs	
Fall time (Notes 1 & 2)		t_f	-	4	6	n secs	

*Measured under pulsed conditions. Width = 300μs. Duty cycle ≤ 2%.

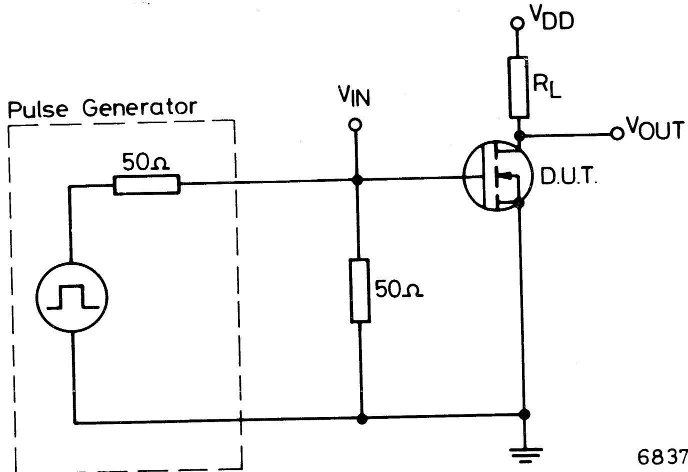
Note 1 Switching times measured with 50 ohm source impedance and <5ns rise time on a pulse generator.

Note 2 Sample test.

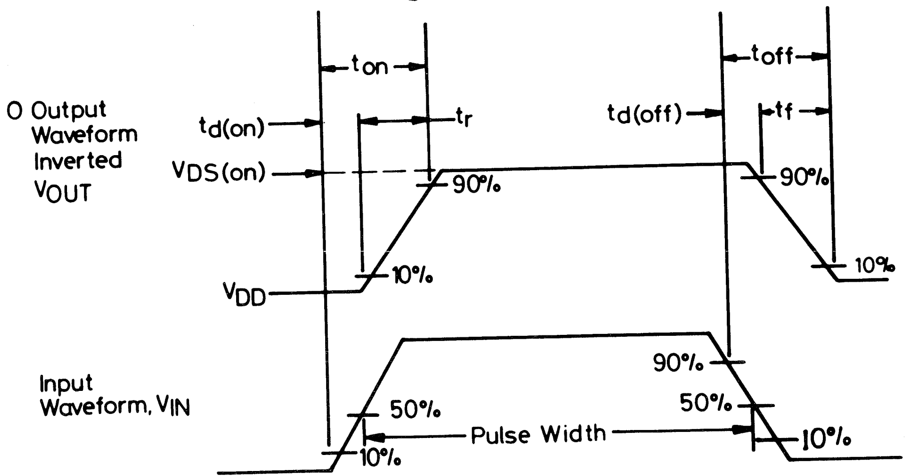
DRAIN-SOURCE DIODE CHARACTERISTICS

Parameter	Symbol	Typ.	Unit	Conditions
Forward ON voltage*	V_{SD}	0.77	V	$V_{GS}=0$, $I_S=0.1A$

Circuit for Measuring Switching Times



Switching Waveforms



Input voltage amplitude 10 Volts peak

Note:
Power MOSFET switching times are essentially independent of operating temperature

6838/1

Fig. 1 Output Characteristics

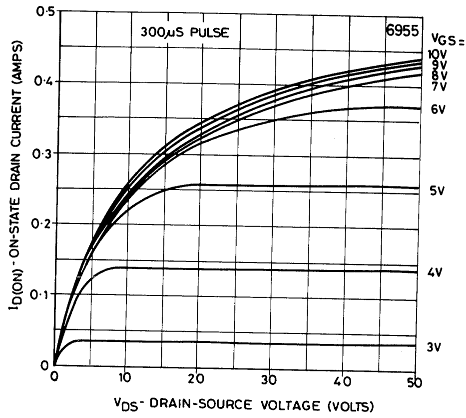


Fig. 2 Saturation Characteristics

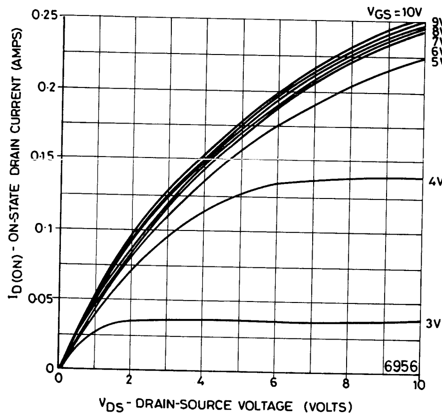


Fig. 3 Voltage Saturation Characteristics

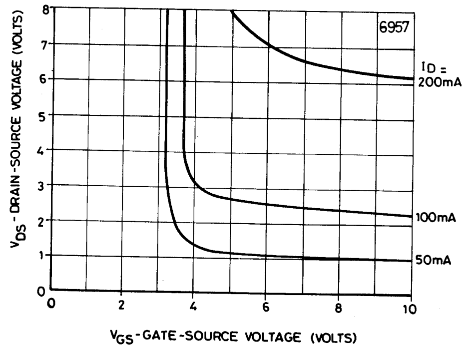


Fig. 4 Transfer Characteristics

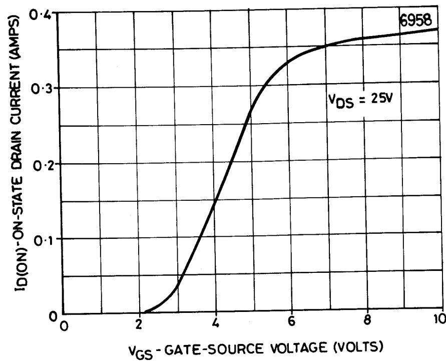


Fig. 5 Capacitance vs Drain-Source Voltage

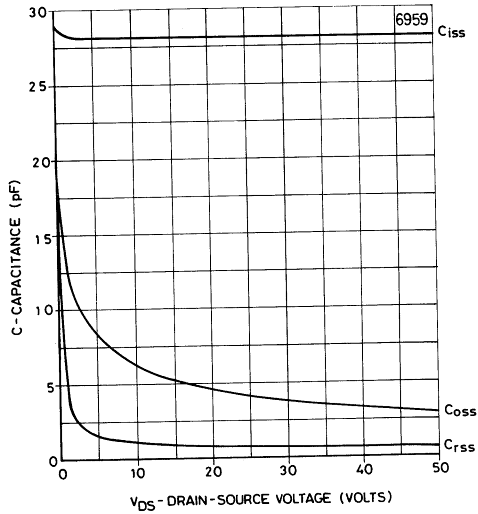


Fig. 6 Transconductance vs Drain-Current

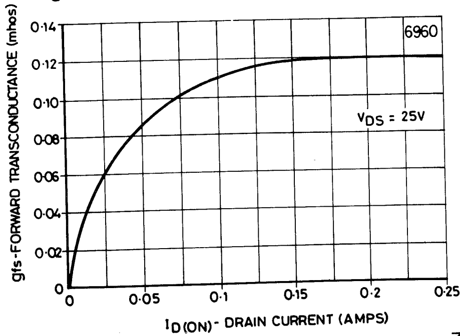


Fig. 7 Transconductance vs Gate-Source Voltage

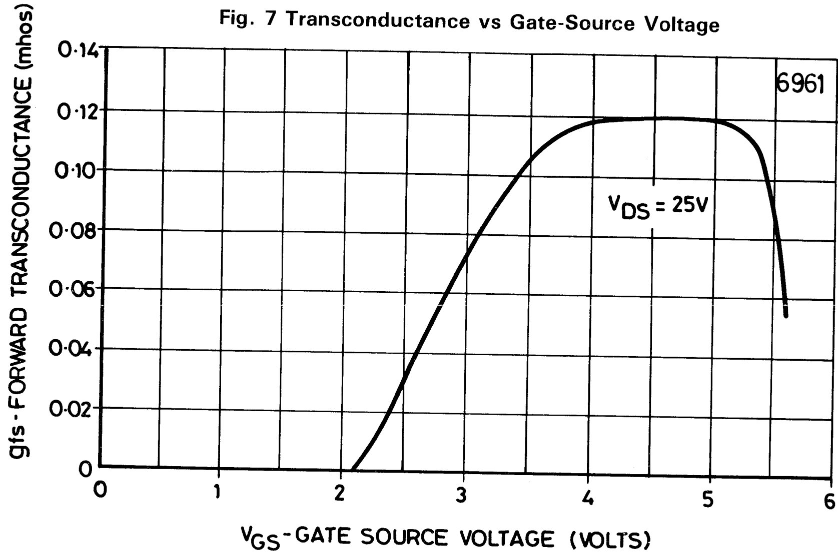


Fig. 8 Gate Charge vs Gate-Source Voltage

V_{DD} = 50V 100V 180V

6962

I_D = 150mA

V_{DD} =

180V 50V, 100V

V_{GS} - GATE-SOURCE VOLTAGE (VOLTS)

16 14 12 10 8 6 4 2 0

0 0·2 0·4 0·6 0·8 1·0 1·2

Q - GATE CHARGE (nC)

Fig. 9 ON-Resistance vs Gate-Source Voltage

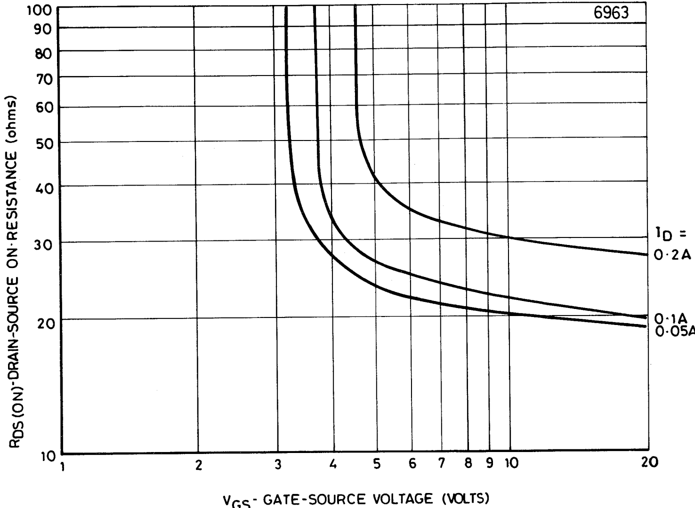
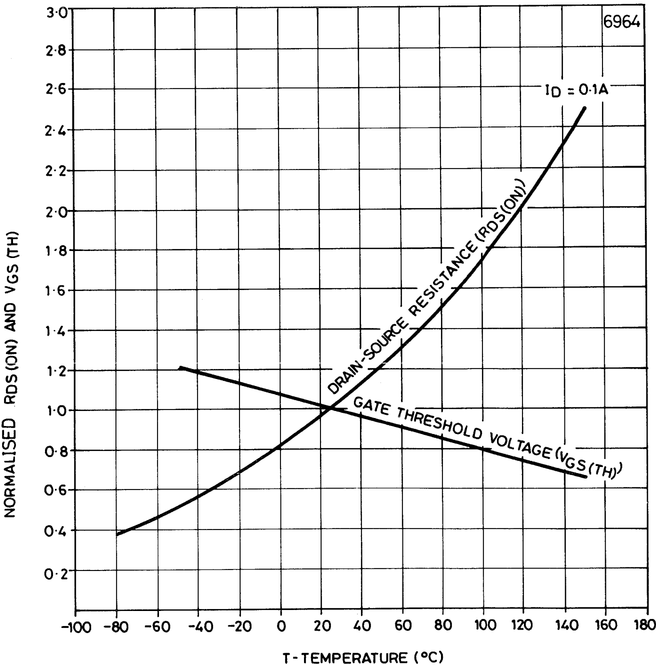
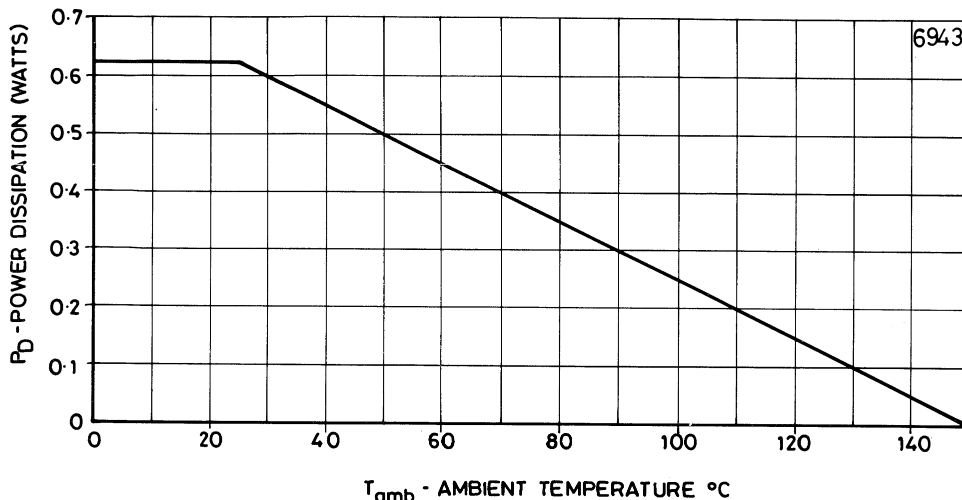


Fig. 10 Variation of $R_{DS(ON)}$ and $V_{GS(th)}$ with Temperature



ZVN3315A/1320A

Fig. 11 Power Derating (Ambient)



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Issue 1, May 1984 4.5M

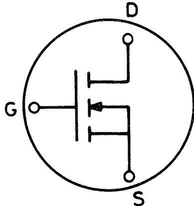
Printed in England CP

ZVN3315B
ZVN1320B

FERRANTI semiconductors®

N-Channel Enhancement-Mode Vertical DMOS Power FET

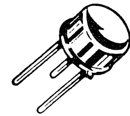
200V: 40 ohm: 0.25A



N-Channel

FEATURES

- Compact Geometry
- Fast Switching Speeds
- No Secondary Breakdown
- Excellent Temperature Stability
- High Input Impedance
- Low Current Drive
- Ease of Paralleling



TO-39 PACKAGE

DESCRIPTION

Compact OVERLAY (CELL) and INTER-DIGITATED geometries are the basis of the new generation of FERRANTI Power MOSFET transistors. These efficient geometries, optimised for low ON-resistance, low capacitances and fast switching speeds, with computer controlled processing combine to achieve greater device ruggedness.

The planar construction, coupled with ion implantation and the self-aligned poly-silicon gate manufacturing process, provides the reliability and stability in performance required in todays designs.

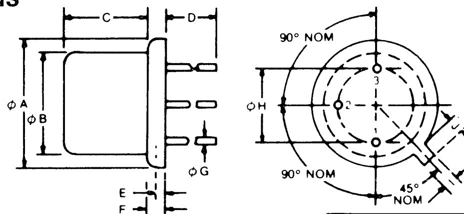
PRODUCT SUMMARY

Device Type	BV_{DSS}	$I_{D(CONT)}$	$R_{D(ON)}$
ZVN3315B	150V	0.25A	40Ω
ZVN1320B	200V	0.25A	40Ω

Chip Size 0.030″ × 0.030″

FERRANTI Power MOSFETS will directly interface with MICROPROCESSORS, LOGIC ARRAYS and standard IC LOGIC families including CMOS, TTL, PMOS and NMOS.

PACKAGE DIMENSIONS



PIN OUT	
1	Source
2	Gate
3	Drain & Case

SYMBOL	INCHES		MILLIMETRES	
	MIN	MAX	MIN	MAX
φA	350	370	8 89	9 40
φB	306	335	7 77	8 51
C	240	260	6 10	6 60
D	500		12 70	
E	009	023	229	584
F	.018	.045	458	1 143
φG	.016	021	406	.533
φH	.190	210	4 83	5.33
I	.028	.037	711	939
J	.026	.040	660	1.016

ZVN3315B/1320B

ABSOLUTE MAXIMUM RATINGS

Parameters		ZVN3315B	ZVN1320B	Units
V_{DS}	Drain-source voltage	150	200	V
I_D	Continuous drain current (@ $T_A=25°C$)	0.1		A
I_D	Continuous drain current (@ $T_C=25°C$)	0.25		A
I_{DM}	Pulse drain current	1		A
V_{GS}	Gate-source voltage	±20		V
P_D	Max. power dissipation (@ $T_A=25°C$)	0.625		W
P_D	Max. power dissipation (@ $T_C=25°C$)	5		W
	Operating/Storage Temperature Range	−55 to +150		°C

ELECTRICAL CHARACTERISTICS (at T=25°C unless otherwise stated)

Parameter		Symbol	Min.	Typ.	Max.	Unit	Conditions
Drain source breakdown voltage	ZVN3315B	BV_{DSS}	150	-	-	V	$I_D=1mA$, $V_{GS}=0$
	ZVN1320B		200	-	-		
Gate-source threshold voltage		$V_{GS(th)}$	1	-	3	V	$I_D=1mA$, $V_{DS}=V_{GS}$
Gate body leakage		I_{GSS}	-	0.1	100	nA	$V_{GS}=\pm20V$, $V_{DS}=0$
Zero gate voltage Drain current (Note 2)		I_{DSS}	-	-	10	μA	V_{DS}=max. rating, $V_{GS}=0$
			-	-	0.05	mA	$V_{DS}=0.8\times$ max. rating $V_{GS}=0$ (T=125°C)
On-state drain current*		$I_{D(ON)}$	0.25	0.37	-	A	$V_{DS}=25V$, $V_{GS}=10V$
Static drain-source ON-resistance*		$R_{DS(ON)}$	-	22	40	Ω	$I_D=0.1A$, $V_{GS}=10V$
Forward transconductance* (Note 2)		g_{fs}	0.075	0.11	-	S	$V_{DS}=25V$, $I_D=0.1A$
Input capacitance (Note 2)		C_{iss}	-	28	45	pF	$V_{DS}=25V$
Common source output capacitance (Note 2)		C_{oss}	-	14	18		$V_{GS}=0$
Reverse transfer capacitance (Note 2)		C_{rss}	-	2	5		f=1MHz
Turn-ON delay time (Notes 1 & 2)		$t_{d(on)}$	-	3	5	n secs	$V_{DD}=25V$
Rise time (Notes 1 & 2)		t_r	-	5	7		
Turn-OFF delay time (Notes 1 & 2)		$t_{d(off)}$	-	4	6		$I_D=0.1A$
Fall time (Notes 1 & 2)		t_f	-	4	6		

*Measured under pulsed conditions. Width=300μs. Duty cycle ≤2%.

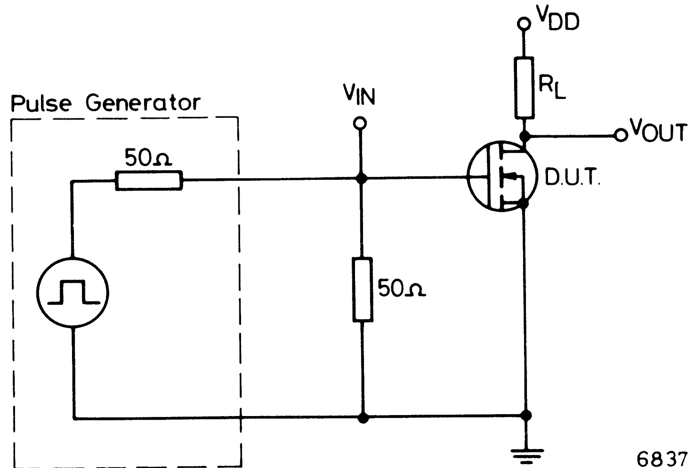
Note 1 Switching times measured with 50 ohm source impedance and <5ns rise time on a pulse generator.

Note 2 Sample test.

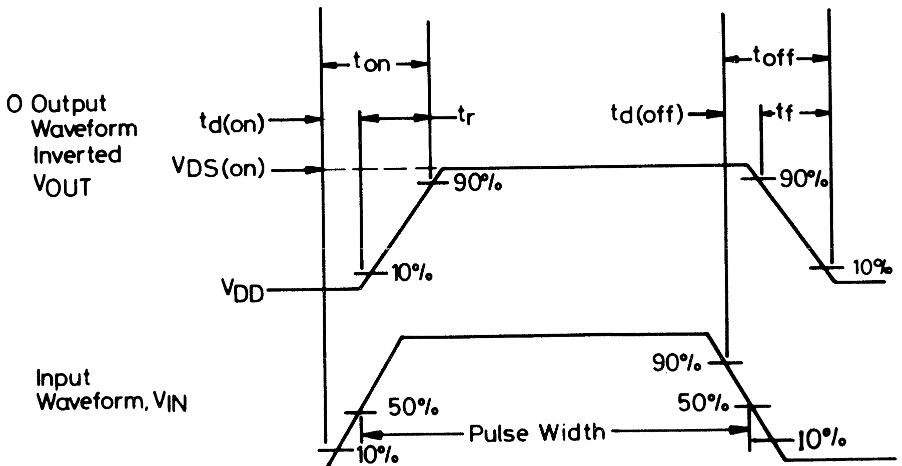
DRAIN-SOURCE DIODE CHARACTERISTICS

Parameter	Symbol	Typ.	Unit	Conditions
Forward ON voltage*	V_{SD}	0.83	V	$V_{GS}=0$, $I_S=0.25A$

Circuit for Measuring Switching Times



Switching Waveforms



Input voltage amplitude 10 Volts peak

Note:
Power MOSFET switching times are essentially independent of operating temperature

6838/1

Fig. 1 Output Characteristics

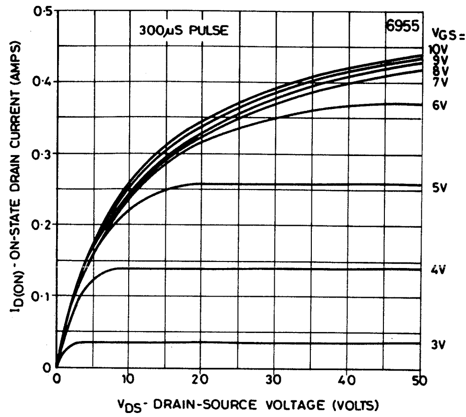


Fig. 2 Saturation Characteristics

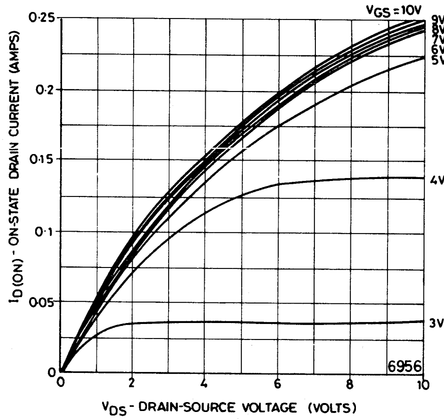


Fig. 3 Voltage Saturation Characteristics

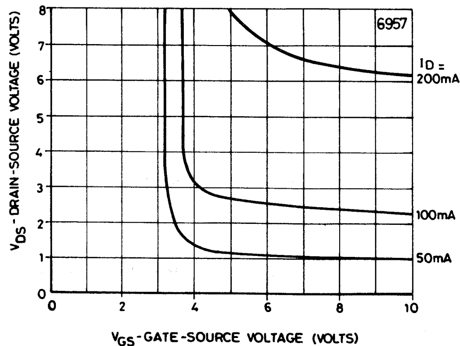


Fig. 4 Transfer Characteristics

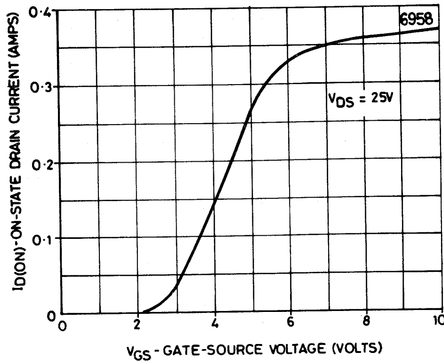


Fig. 5 Capacitance vs Drain-Source Voltage

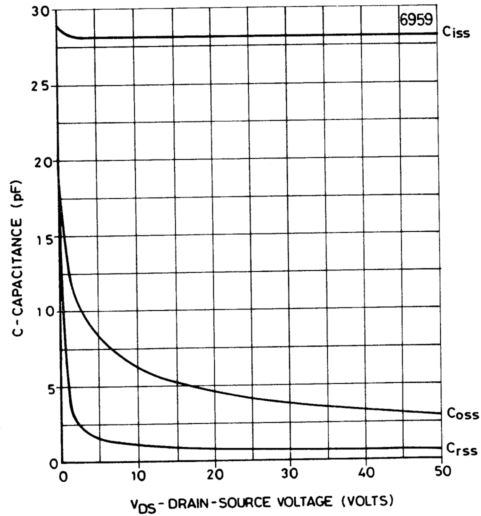


Fig. 6 Transconductance vs Drain-Current

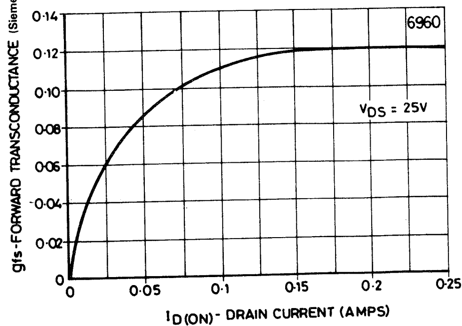


Fig. 7 Transconductance vs Gate-Source Voltage

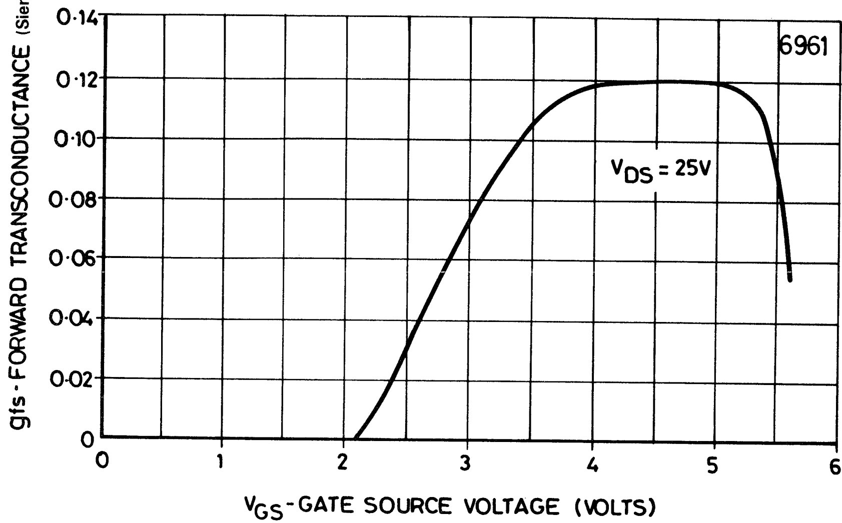


Fig. 8 Gate Charge vs Gate-Source Voltage

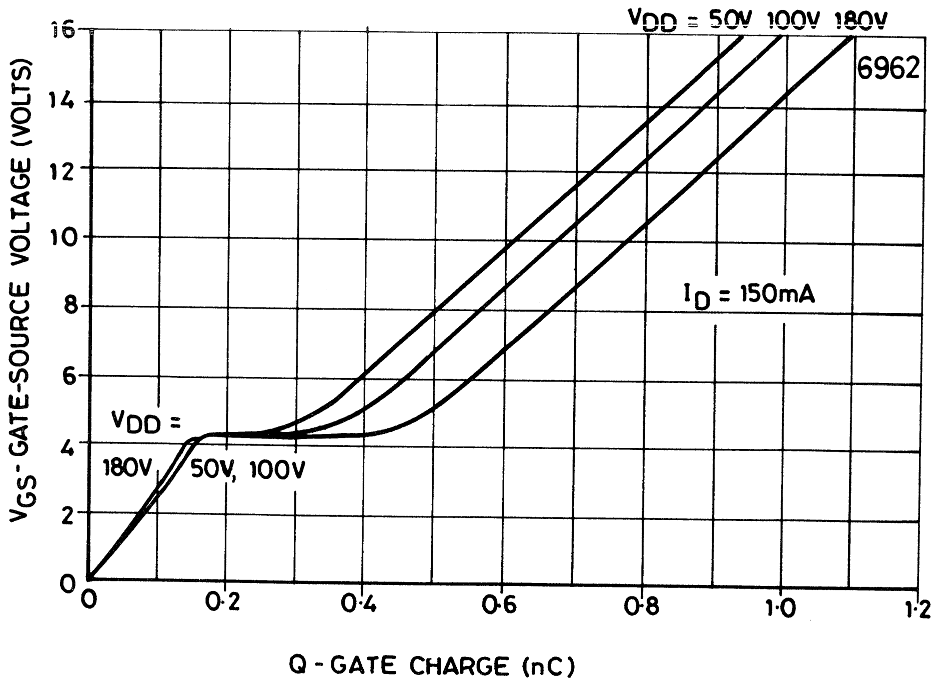


Fig. 9 ON-Resistance vs Gate-Source Voltage

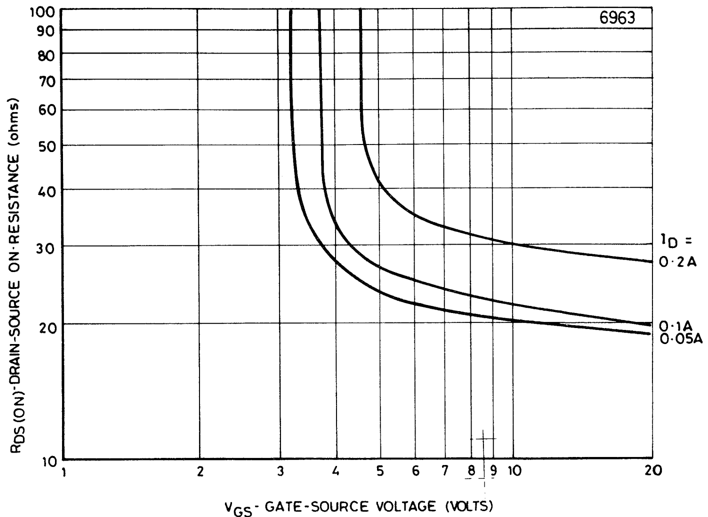
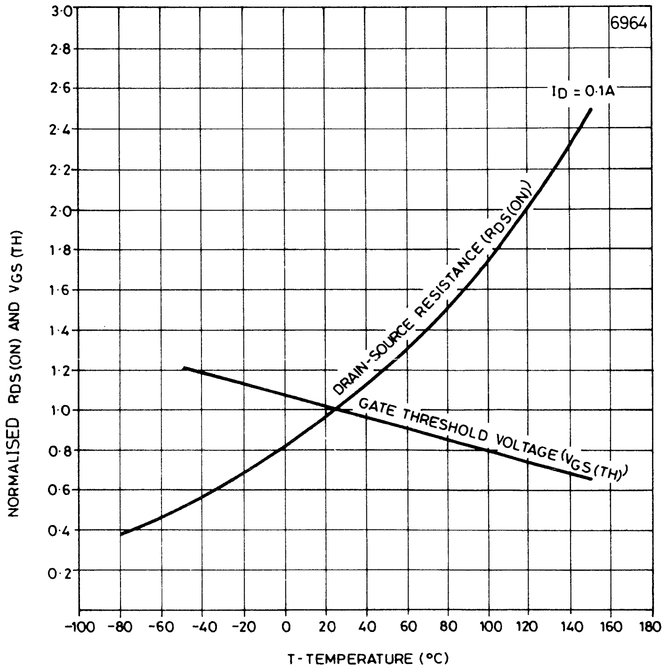


Fig. 10 Variation of $R_{DS(ON)}$ and $V_{GS(th)}$ with Temperature



ZVN3315B/1320B

Fig. 11 Power Derating (Ambient)

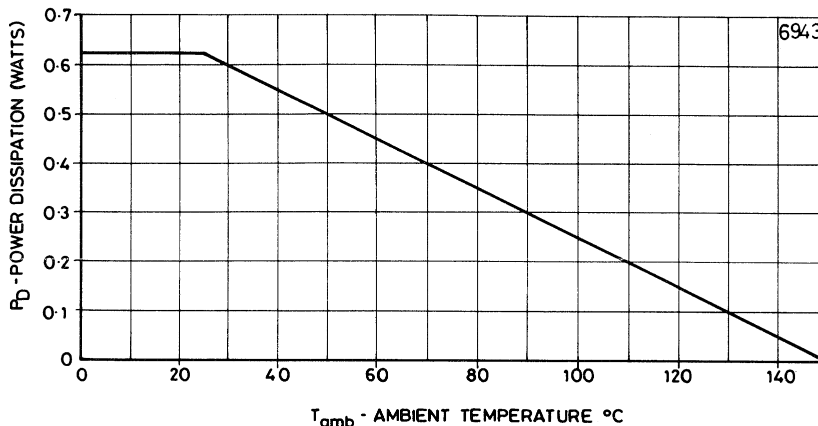
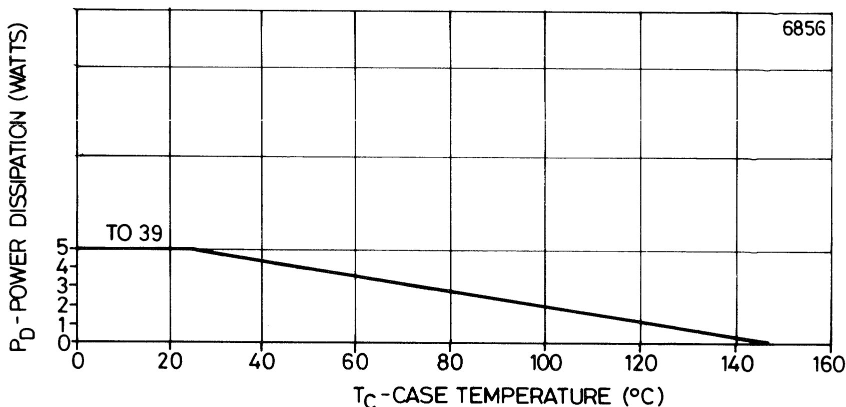


Fig. 12 Power Derating (Case)



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Issue 1, August 1984 5.1M

Section 6

ZVN14 Range

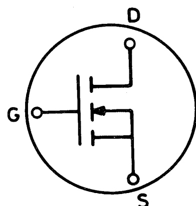
ZVN1409A

ZVN1404A
ZVN1406A
ZVN1408A
ZVN1409A

FERRANTI semiconductors®

N-Channel Enhancement-Mode Vertical DMOS FET

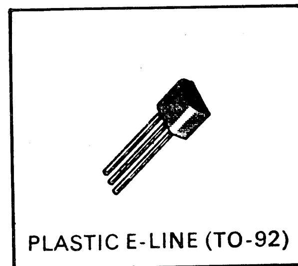
90V: 250 ohm: 10mA



N-Channel

FEATURES

- Compact Geometry
- Very Fast Switching Speeds
- No Secondary Breakdown
- Excellent Temperature Stability
- High Input Impedance
- Low Current Drive
- Ease of Paralleling



PLASTIC E-LINE (TO-92)

DESCRIPTION

Compact OVERLAY (CELL) and INTER-DIGITATED geometries are the basis of the new generation of FERRANTI Power MOSFET transistors. These efficient geometries, optimised for low ON-resistance, low capacitances and fast switching speeds, with computer controlled processing combine to achieve greater device ruggedness.

The planar construction, coupled with ion implantation and the self-aligned poly-silicon gate manufacturing process, provides the reliability and stability in performance required in todays designs.

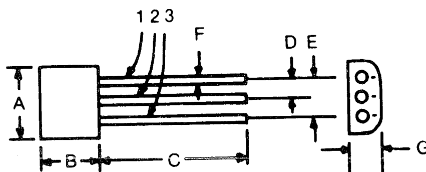
PRODUCT SUMMARY

Device Type	BV_{DSS}	$I_{D(CONT)}$	$R_{D(ON)}$
ZVN1404A	40V	10mA	250Ω
ZVN1406A	60V	10mA	250Ω
ZVN1408A	80V	10mA	250Ω
ZVN1409A	90V	10mA	250Ω

Chip Size 0.012″ × 0.019″

FERRANTI Power MOSFETS will directly interface with MICROPROCESSORS, LOGIC ARRAYS and standard IC LOGIC families including CMOS, TTL, PMOS and NMOS.

PACKAGE DIMENSIONS



PIN OUT	
1	Drain
2	Gate
3	Source

SYMBOL	INCHES		MILLIMETRES	
	MIN	MAX	MIN	MAX
A	.172	.188	4.37	4.77
B	.142	.158	3.61	4.01
C	.475	.525	12.06	13.34
D	.05		1.27	
E	.10		2.54	
F	.016	.019	.406	.495
G	.085	.095	2.16	2.42

Also available with various lead bends and on tape and reel.

ZVN1404A/1406A/1408A/1409A

ABSOLUTE MAXIMUM RATINGS

	Parameters	ZVN1404A	ZVN1406A	ZVN1408A	ZVN1409A	Units
V_{DS}	Drain-source voltage	40	60	80	100	V
I_D	Continuous drain current (@ $T_A=25°C$)	10				mA
I_D	Continuous drain current (@ $T_C=25°C$)	-				A
I_{DM}	Pulse drain current	40				mA
V_{GS}	Gate-source voltage	±20				V
P_D	Max. Power Dissipation (@ $T_A=25°C$)	0.625				W
P_D	Max. Power Dissipation (@ $T_C=25°C$)	-				W
	Operating/Storage Temperature Range	−55 to +150				°C

ELECTRICAL CHARACTERISTICS (at T=25°C unless otherwise stated)

Parameter		Symbol	Min.	Typ.	Max.	Unit	Conditions
Drain source breakdown voltage	ZVN1404A	BV_{DSS}	40	-	-	V	$I_D=0.1mA$ $V_{GS}=0$
	ZVN1406A		60	-	-		
	ZVN1408A		80	-	-		
	ZVN1409A		90	-	-		
Gate-source threshold voltage		$V_{GS(th)}$	0.8	-	2.4	V	$I_D=0.1mA$, $V_{DS}=V_{GS}$
Gate body leakage		I_{GSS}	-	1	100	nA	$V_{GS}=\pm20V$, $V_{DS}=0$
Zero gate voltage Drain current (Note 2)		I_{DSS}	-	-	1	µA	V_{DS}=max. rating, $V_{GS}=0$
			-	-	100	µA	$V_{DS}=0.8\times$ max. rating $V_{GS}=0$ $(T=125°C)$
On-state drain current*		$I_{D(ON)}$	10	25	-	mA	$V_{DS}=25V$, $V_{GS}=10V$
Static drain-source ON-resistance*		$R_{DS(ON)}$	-	200	250	Ω	$I_D=5mA$, $V_{GS}=10V$
Forward transconductance* (Note 2)		g_{fs}	2	3	-	mS	$V_{DS}=25V$, $I_D=10mA$
Input capacitance (Note 2)		C_{iss}	-	6	6.5	pF	$V_{DS}=25V$ $V_{GS}=0$ $f=1MHz$
Common source output capacitance (Note 2)		C_{oss}	-	2.5	3		
Reverse transfer capacitance (Note 2)		C_{rss}	-	0.4	0.5		
Turn-ON delay time (Notes 1 & 2)		$t_{d(on)}$	-	0.3	-	n secs	$V_{DD}=25V$ $I_D\simeq5mA$ $R_L=1k\Omega$ $V_G=10V$ peak
Rise time (Notes 1 & 2)		t_r	-	0.5	-		
Turn-OFF delay time (Notes 1 & 2)		$t_{d(off)}$	-	0.35	-		
Fall time (Notes 1 & 2)		t_f	-	0.5	-		

* Measured under pulsed conditions. Width=300µs. Duty cycle ≤2%.
Note 1 Switching times tend to be dominated by associated circuitry.
Note 2 Sample test.

Fig. 1 Saturation Characteristics

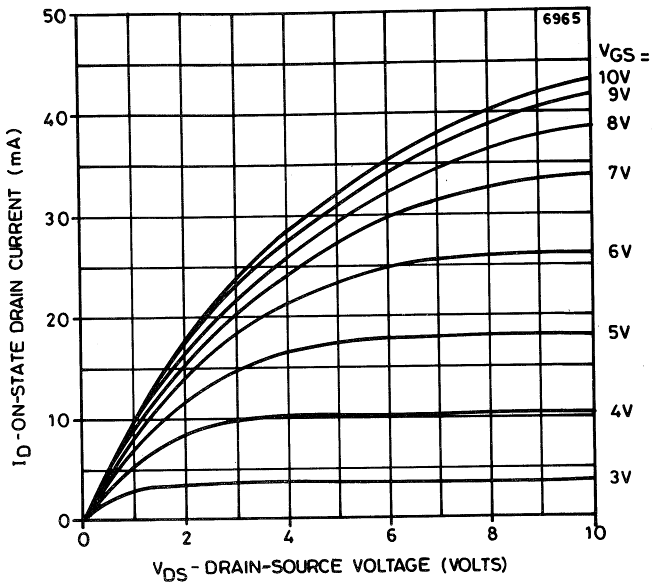


Fig. 2 Voltage Saturation Characteristics

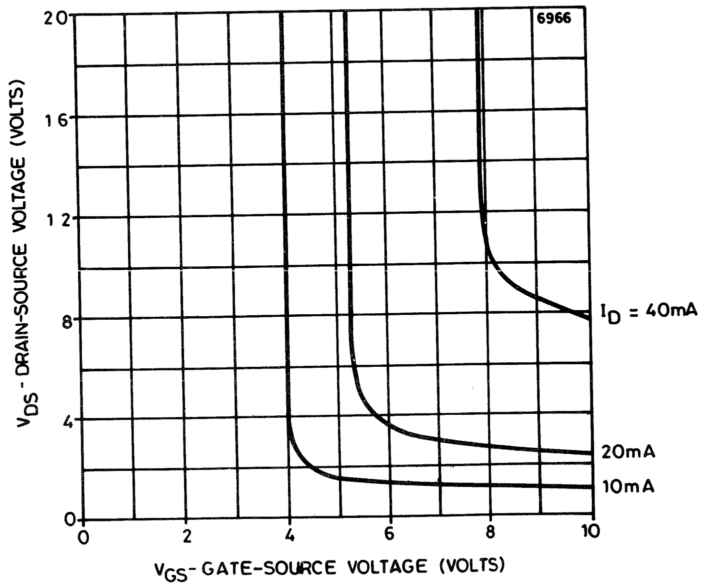


Fig. 3 Transfer Characteristics

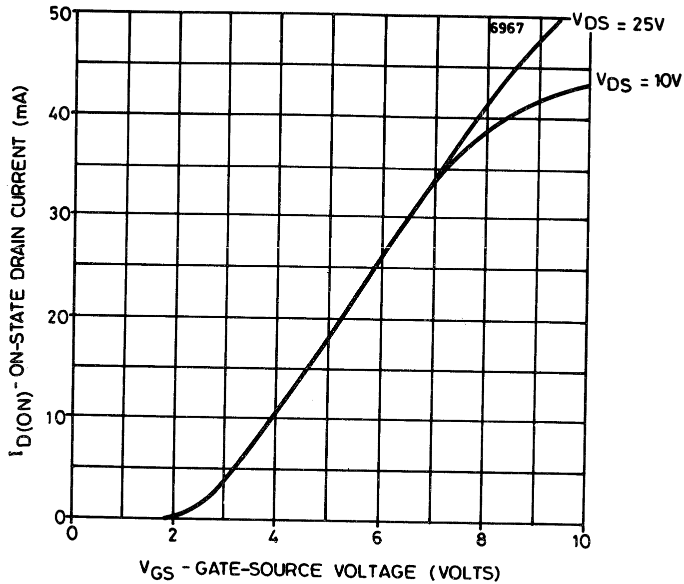


Fig. 4 Capacitance vs Drain-Source Voltage

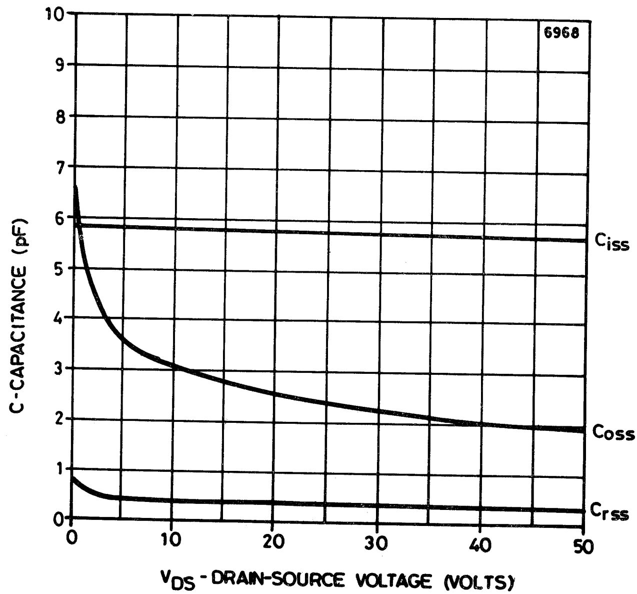


Fig. 5 Transconductance vs Drain Current

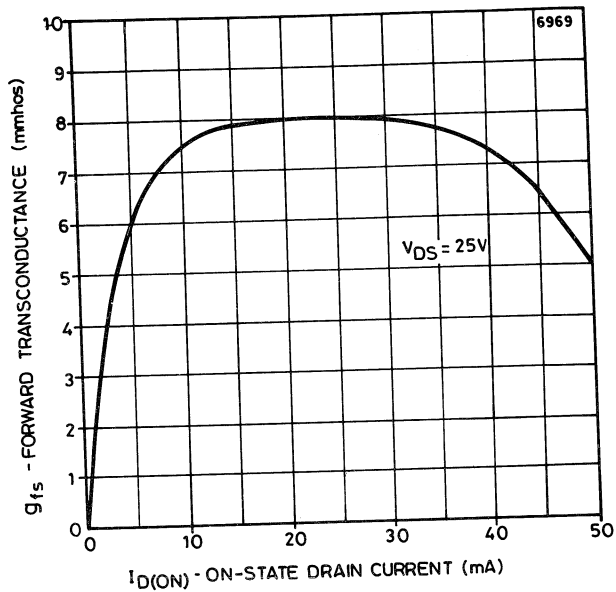
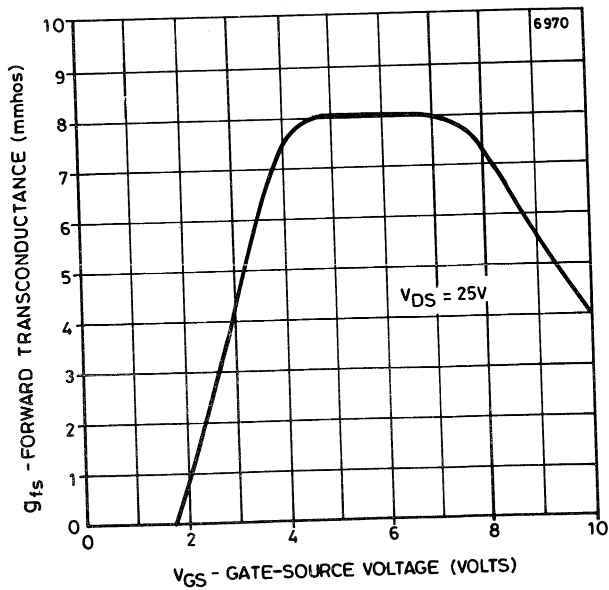


Fig. 6 Transconductance vs Gate-Source Voltage



ZVN1404A/1406A/1408A/1409A

Fig. 7 ON-Resistance vs Gate-Source Voltage

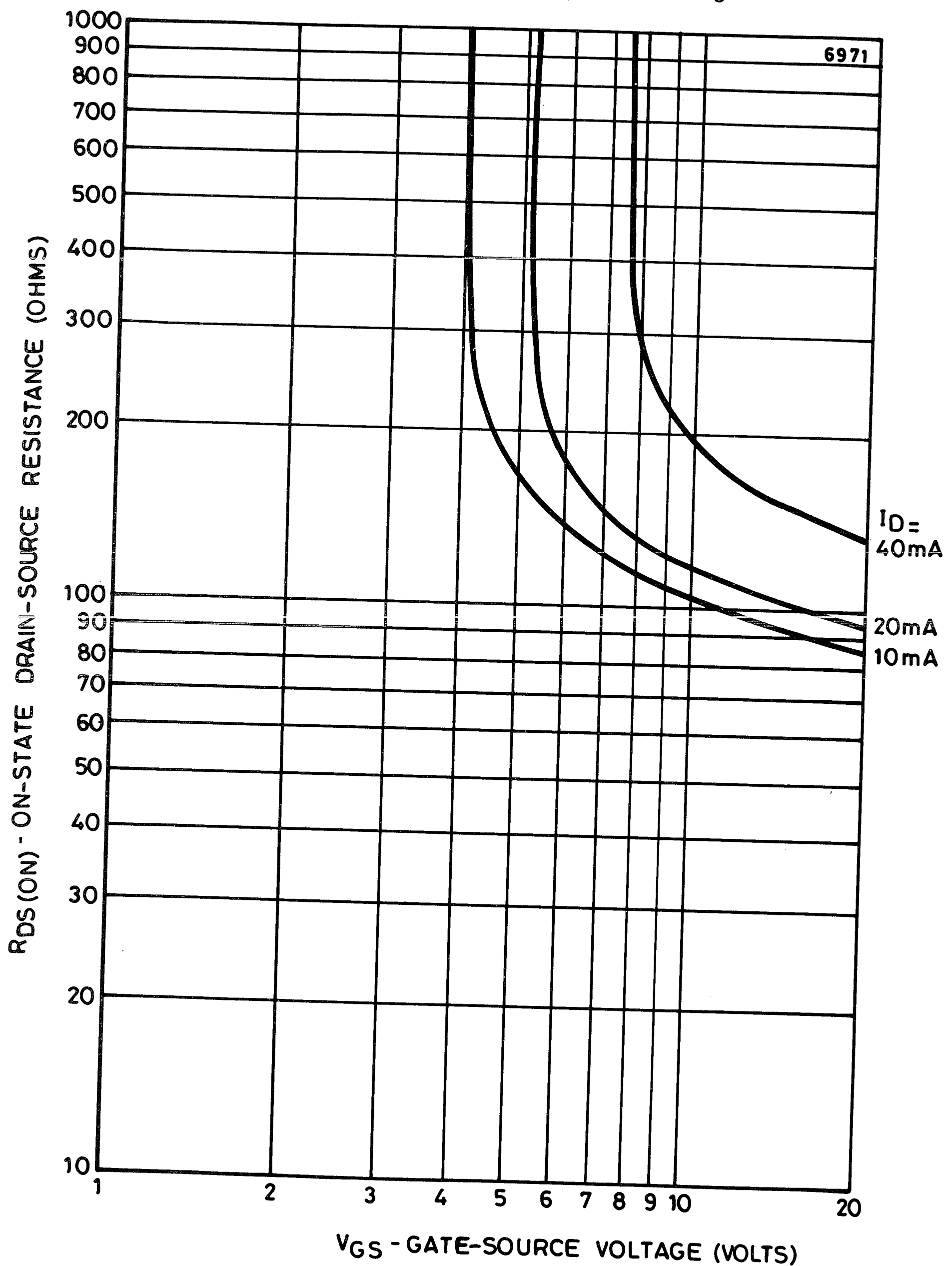


Fig. 8 Variation of $R_{DS(ON)}$ and $V_{GS(th)}$ with Temperature

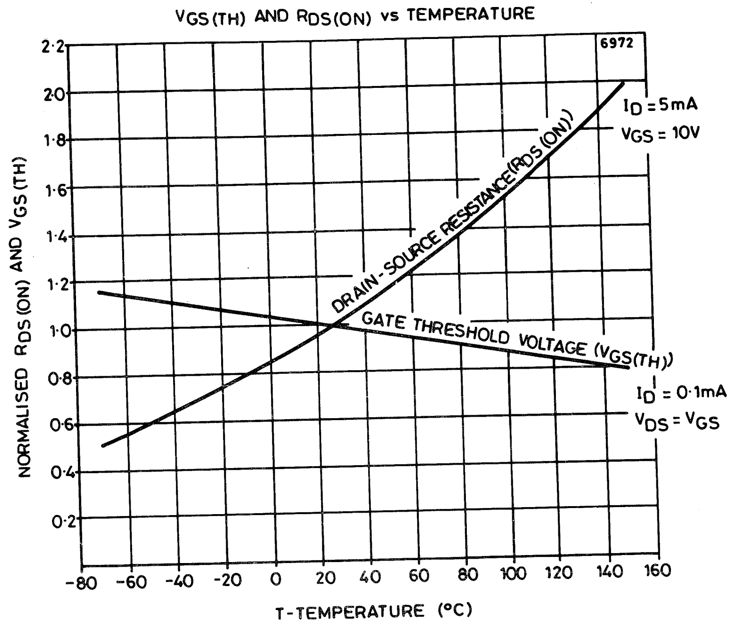
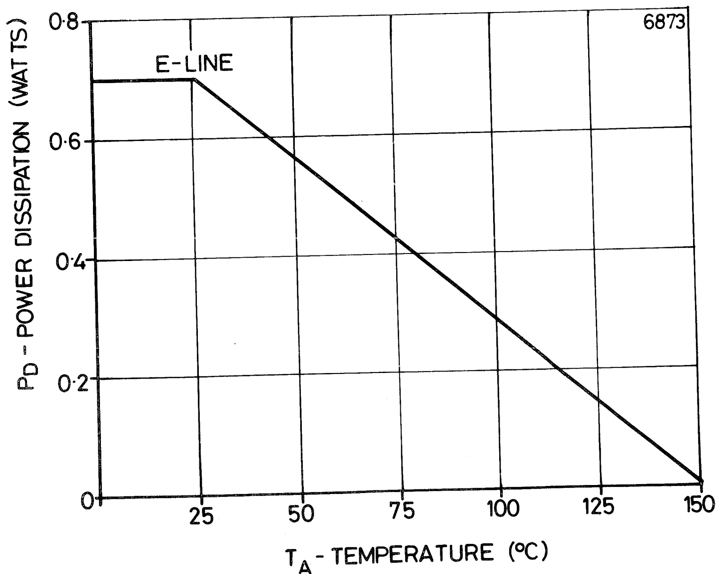


Fig. 9 Power Derating (Ambient)



ZVN1404A/1406A/1408A/1409A

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Issue 1, May 1984 4.5M

Printed in England CP

P-CHANNEL DEVICES

P-CHANNEL MOSFET SELECTION GUIDE

BV_{DSS} V Min.	$R_{DS(ON)}$ Ω Max. @	I_D A	Device	$I_{D(cont)}$ A Max.	P_D W	Package
350	100	0.05	ZVP0535A	0.05	0.7	E-Line
			ZVP0535B	0.14	5	TO-39
			ZVP0535L	0.28	20	TO-220
300			ZVP0530A	0.05	0.7	E-Line
			ZVP0530B	0.14	5	TO-39
			ZVP0530L	0.28	20	TO-220
200	80	0.07	ZVP1320A	0.07	0.625	E-Line
			ZVP1320B	0.19	5	TO-39
	32	0.1	ZVP0120A	0.11	0.7	E-Line
			ZVP0120B	0.25	5	TO-39
			ZVP0120L	0.25	20	TO-220
	12	0.5	ZVP2220B	1.0	20	TO-39
			ZVP2220L	1.0	20	TO-220
150	80	0.07	ZVP3315A	0.07	0.625	E-Line
			ZVP3315B	0.19	5	TO-39
	32	0.1	ZVP2115A	0.11	0.7	E-Line
			ZVP2115B	0.25	5	TO-39
			ZVP2115L	0.25	20	TO-220
	12	0.5	ZVP2215B	1.0	20	TO-39
			ZVP2215L	1.0	20	TO-220
100	20	0.2	ZVP3310A	0.14	0.625	E-Line
			ZVP3310B	0.38	5	TO-39
	8	0.5	ZVP2110A	0.23	0.7	E-Line
			ZVP2110B	0.6	5	TO-39
			ZVP2110L	0.75	20	TO-220
	3	0.75	ZVP2210B	1.5	20	TO-39
			ZVP2210L	1.5	20	TO-220
80	20	0.2	ZVP1308A	0.14	0.625	E-Line
			ZVP1308B	0.38	5	TO-39
	8	0.5	ZVP0108A	0.23	0.7	E-Line
			ZVP0108B	0.6	5	TO-39
			ZVP0108L	0.75	20	TO-220
	3	0.75	ZVP2208B	1.5	20	TO-39
			ZVP2208L	1.5	20	TO-220

P-CHANNEL MOSFET SELECTION GUIDE

BV_{DSS} V Min.	$R_{DS(ON)}$ Ω Max.	@ I_D A	Device	$I_{D(cont)}$ A Max.	P_D W	Package
60	20	0.2	ZVP1306A	0.14	0.625	E-Line
			ZVP1306B	0.38	5	TO-39
	14	0.37	ZVP3306A	0.16	0.625	E-Line
			ZVP3306B	0.46	5	TO-39
		0.2	BS250P	0.50	0.7	E-Line
	8	0.5	ZVP0106A	0.23	0.7	E-Line
			ZVP0106B	0.6	5	TO-39
			ZVP0106L	0.75	20	TO-220
	5		ZVP2106A	0.28	0.7	E-Line
			ZVP2106B	0.76	5	TO-39
			ZVP2106L	1.0	20	TO-220
	1.5	1	ZVP2206B	2.0	20	TO-39
			ZVP2206L	2.0	20	TO-220
40	14	0.37	ZVP3304A	0.16	0.625	E-Line
			ZVP3304B	0.46	5	TO-39
	5	0.5	ZVP2104A	0.28	0.7	E-Line
			ZVP2104B	0.76	5	TO-39
			ZVP2104L	1.0	20	TO-220
	1.5	1	ZVP2204B	2.0	20	TO-39
			ZVP2204L	2.0	20	TO-220
20	14	0.37	ZVP3302A	0.16	0.625	E-Line
			ZVP3302B	0.46	5	TO-39
	5	0.5	ZVP0102A	0.28	0.7	E-Line
			ZVP0102B	0.76	5	TO-39
			ZVP0102L	1.0	20	TO-220
	1.5	1	ZVP2202B	2.0	20	TO-39
			ZVP2202L	2.0	20	TO-220

NEW PRODUCTS

NEW PRODUCTS

The following products will be available during 1985. Contact your nearest Ferranti Sales Office for upto date information.

ZVN32 family (Provisional Data)

Device	BV_{DSS} V	$R_{DS(ON)}$ Ω	$I_{D(cont)}$ A	Package
ZVN3202L	20	0.15	14	TO-220
ZVN3204L	40	0.15	14	TO-220
ZVN3206L	60	0.15	14	TO-220
ZVN3208L	80	0.18	14	TO-220
ZVN3210L	100	0.18	14	TO-220
ZVN3215L	150	0.6	9	TO-220
ZVN3220L	200	0.6	9	TO-220

ZVN01/21 family (Provisional Data)

The following devices are to be added to this family.

Device	BV_{DSS} V	$R_{DS(ON)}$ Ω	$I_{D(cont)}$ A	Package
ZVN0124A	240	16	0.16	E-Line
ZVN0124B	240	16	0.42	TO-39
ZVN0124L	240	16	0.5	TO-220
ZVN2120A	200	10	0.17	E-Line
ZVN2120B	200	10	0.46	TO-39
ZVN2120L	200	10	0.5	TO-220
ZVN2117A	170	10	0.17	E-Line
ZVN2117B	170	10	0.46	TO-39
ZVN2117L	170	10	0.5	TO-220

NEW PRODUCTS

The ZVN05/25 (Provisional Data)

The following devices are to be added to this family.

Device	BV_{DSS} V	$R_{DS(ON)}$ Ω	$I_{D(cont)}$ A	Package
ZVN2535A	350	35	0.09	E-Line
ZVN2535B	350	35	0.24	TO-39
ZVN2535L	350	35	0.48	TO-220
ZVN2530A	300	35	0.09	E-Line
ZVN2530B	300	35	0.24	TO-39
ZVN2530L	300	35	0.48	TO-220

MOSFETs in SOT-23 (Provisional Data)

1. N-channel

Device	BV_{DSS} V	$R_{DS(ON)}$ Ω	$I_{D(cont)}$ A	Package
ZVN1320F	200	40	0.05	SOT-23
ZVN3315F	150	40	0.05	SOT-23
ZVN3310F	100	10	0.10	SOT-23
ZVN1308F	80	10	0.10	SOT-23
ZVN1306F	60	10	0.10	SOT-23
ZVN3306F	60	5	0.15	SOT-23
ZVN3304F	40	5	0.15	SOT-23
ZVN3302F	20	5	0.15	SOT-23

NEW PRODUCTS

1. P-channel

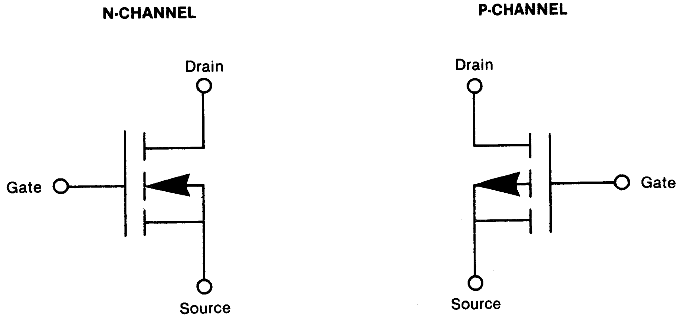
Device	BV_{DSS} V	$R_{DS(ON)}$ Ω	$I_{D(cont)}$ A	Package
ZVP1320F	200	80	0.035	SOT-23
ZVP3315F	150	80	0.035	SOT-23
ZVP3310F	100	20	0.075	SOT-23
ZVP1308F	80	20	0.075	SOT-23
ZVP1306F	60	20	0.075	SOT-23
ZVP3306F	60	14	0.090	SOT-23
ZVP3304F	40	14	0.090	SOT-23
ZVP3302F	20	14	0.090	SOT-23

NOTES

NOTES

GLOSSARY OF TERMS

GLOSSARY OF TERMS



Device Schematics

Symbol	Parameter	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	V
C	Capacitance	F
C_{DS}	Drain-Source Capacitance	F
C_{GD}	Gate-Drain Capacitance	F
C_{GS}	Gate-Source Capacitance	F
C_{iss}	Input Capacitance ($C_{iss} = C_{GD} + C_{GS}$)	F
C_{oss}	Common Source Output Capacitance ($C_{oss} = C_{GD} + C_{DS}$)	F
C_{rss}	Reverse Transfer Capacitance ($C_{rss} = C_{DS}$)	F
f	Frequency	Hz
g_{fs}	Forward Transconductance	S
I_D	Continuous Drain Current	A
I_{DM}	Pulsed Drain Current	A
$I_{D(on)}$	On-State Drain Current	A
I_{DSS}	Zero Gate Voltage Drain Current	A
I_{GSS}	Gate-Body Leakage Current	
P_D	Power Dissipation	W
Q_g	Gate Charge	c
$r_{ds(on)}$	Small Signal Drain-Source On-State Resistance	Ω
$R_{DS(on)}$	Static Drain-Source On-State Resistance	Ω

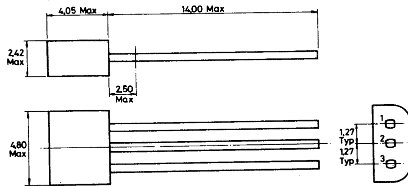
GLOSSARY OF TERMS

Symbol	Parameter	Unit
$t_{d(off)}$	Turn-Off Delay Time	s
$t_{d(on)}$	Turn-On Delay Time	s
t_f	Fall Time	s
t_{off}	Turn-Off Time ($t_{off} = t_d(off) + t_f$)	s
t_{on}	Turn-On Time ($t_{on} = t_{d(on)} + t_r$)	s
t_r	Rise Time	s
T	Temperature	°C
T_A	Ambient Temperature	°C
T_C	Case Temperature	°C
V_{DD}	Drain Drive Voltage	V
V_{DG}	Drain-Gate Voltage	V
V_{DS}	Drain-Source Voltage	V
$V_{DS(on)}$	Drain-Source On Voltage	V
V_{GS}	Gate-Source Voltage	V
$V_{GS(th)}$	Gate Threshold Voltage	V
$\Theta_{j\text{-}a}$	Thermal Resistance Junction to Ambient	°C/W
$\Theta_{j\text{-}c}$	Thermal Resistance Junction to Case	°C/W

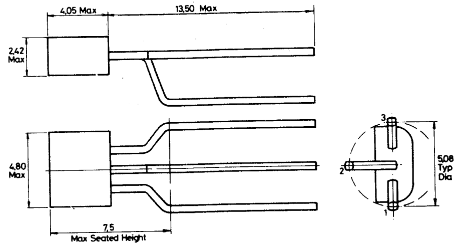
E-LINE PACKAGE OPTIONS
+
TAPING SPECIFICATIONS

E-LINE PACKAGE OPTIONS

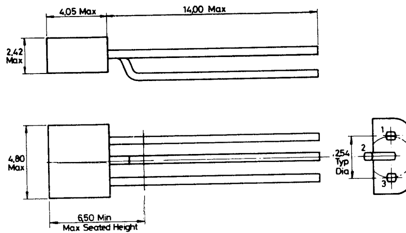
Devices can be ordered with the following lead configurations by adding the indicated suffix to the part number.



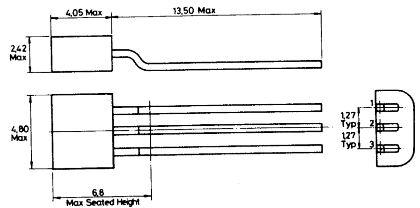
STANDARD PACKAGE
BS 3934.. SO-94



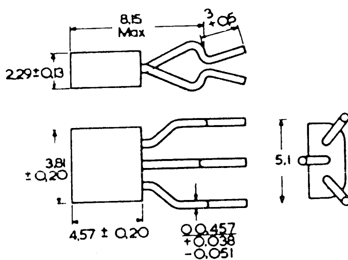
'K' LEAD FORMATION
for TO-5 and TO-39
compatibility
BS 3934.. SO-95



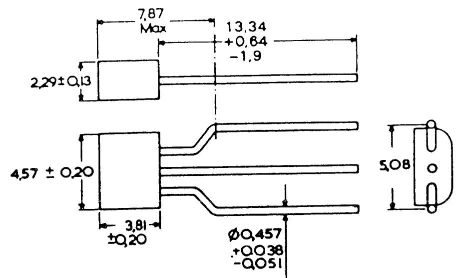
'L' LEAD FORMATION
for TO-18 compatibility
BS 3934.. SO-97



'M' LEAD FORMATION
for flat mounting
BS 3934.. SO-96



'Q' LEAD FORMATION



'S' LEAD FORMATION

TO-92

Dimensions in millimetres

NOTE

The 'S' type lead formation is pin compatible with the popular TO-202.

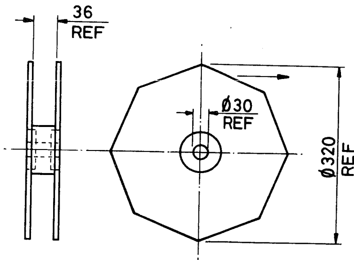
TAPED PRODUCT

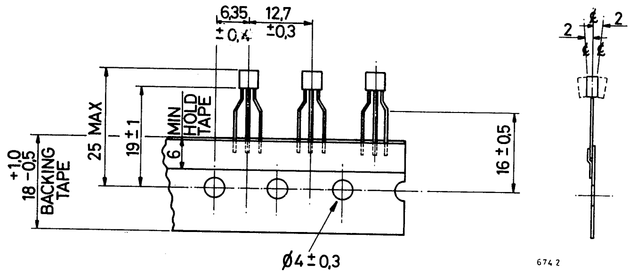
E-Line MOSFETs can be supplied on tape for automatic insertion. Two types of packaging are available:

(a) The tape, bearing the devices, is wound on a reel and supplied in a cardboard box.

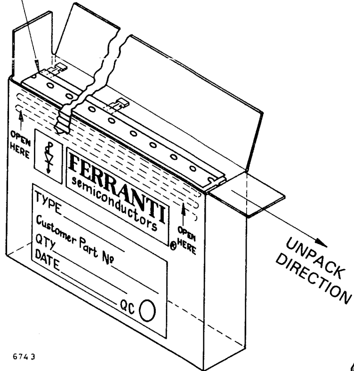
(b) The tape, bearing the devices, is folded in a concertina (or Z) form and supplied in a cardboard box (Ammo Pack).

→ DIRECTION OF UNREELING →





TAPE FOLDED IN CARTON CONCERTINA STYLE



TAPE FEATURES

- Each Reel or Box contains 2000 devices.
- No more than 2 consecutive vacant spaces on the tape.
- Minimum of 5 vacant spaces at beginning and end of tape.
- Available with choice of orientation.

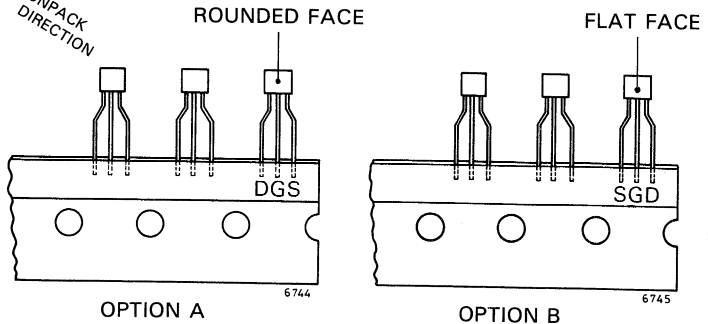
To order E-line MOSFETs on tape, the following format should be used.

(a) Suffix 'STO' for product taped and put on reels.

(b) Suffix 'STZ' for product taped and folded (Ammo Pack).

(c) Orientation (option A or B).

e.g. ZVN0106A STOA.



OPTION A

OPTION B

CUSTOMER SERVICE INFORMATION

Our Customer Service i enquires. The services we offer are d

DELIVERY ENQUIRIES, **11-624 0515**

Information on the curre ill be given by members of our staff w

Rode Kruislaan 119 – 5628 GD Eindhoven
Postbus 1052 – 5602 BB Eindhoven
Telefoon 040-421191 – Telex 59083

In the Sales Department ... you with price quotations and with technical advice on problems relating to your individual requirements. These engineers are assigned to specific areas and are thus familiar with many of your company's needs. They are also in constant touch with our **Field Sales Engineers** who will be pleased to call upon you to discuss your semiconductor requirements.

DISTRIBUTORS

Orders under £100 in value are dealt with by our distributors, whose addresses are shown below under their geographical areas.

The distributor's area is **not** limited to his geographical location.

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Ferranti Wheelock Microelectronics Limited, 65 Wong Chuk Hang Road
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